

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG ,CPU-Memory	3,4
CPU-Power,CPU-GND	5,6
SO_DDRIII DIMMA1&SO_DDRIII DIMMB1	7,8
PPT-PCI /E/DMI /CLK/USB20/USB30	9
PPT-SATA/HOST/GPIO/VGA/CCMOS	10
PPT-SMB/LPC/AUDIO/RTC/SPI	11
PPT-POWER,GND/NVRAM /CP STRAPS	12,13,14
PCIE Slot	15,16
PCIE To PCI Bri	17
PCI Slot	18
SIO-Fintek F71869AD	19
AUDIO 892/887	20
LAN - RTL8111E/8105	21
DVI /HDMI /VGA/SATA Connector	22,23,24,25
USB2.0/3.0 Connector	26,27
USB FULL CHARGE	28
FAN	28
VRM12 - UT501	29
UP6282 3-Phase+MOS CPU	30
UP6282 1-Phase+MOS GPU	31
UP1513 - VTT POWER	32
OP+MOS - SA POWER	33
UP1513 - DDR POWER	34
UP1513 - PCH POWER	35
ATX F_Panel/EMI /TPM	36
ACPI Controller UPI	37
XDP / Manual Parts	38
EMI CAP	39

MS-7758

Intel -MahoBay plamform H77

ATX

Ver: 10(304.8x243.84)

CPU:

System Chipset:

IVY bridge LGA1155

Panther Point H77(CO-LAY Z77)

Onboard Chip:

HD Audio Codec:ALC892 colay 887

LAN-RTL8111E colay8105E

SIO:Fintek F71868AD

Flash ROM: SPI 64 MB

Main Memory:

DDRIII (1066/1333/1600MHz) * 4 (Dual Channel)

ACPI:

PWM:

UPI

VRD12 -UT501 3+1 Phase

Expansion Slots:

Other:

PCI Express (X16) Slot * 1

SATA3.0 x2+SATA2.0 x4 (PCH)

PCI Express (X1) Slot * 2

USB2.0 *10

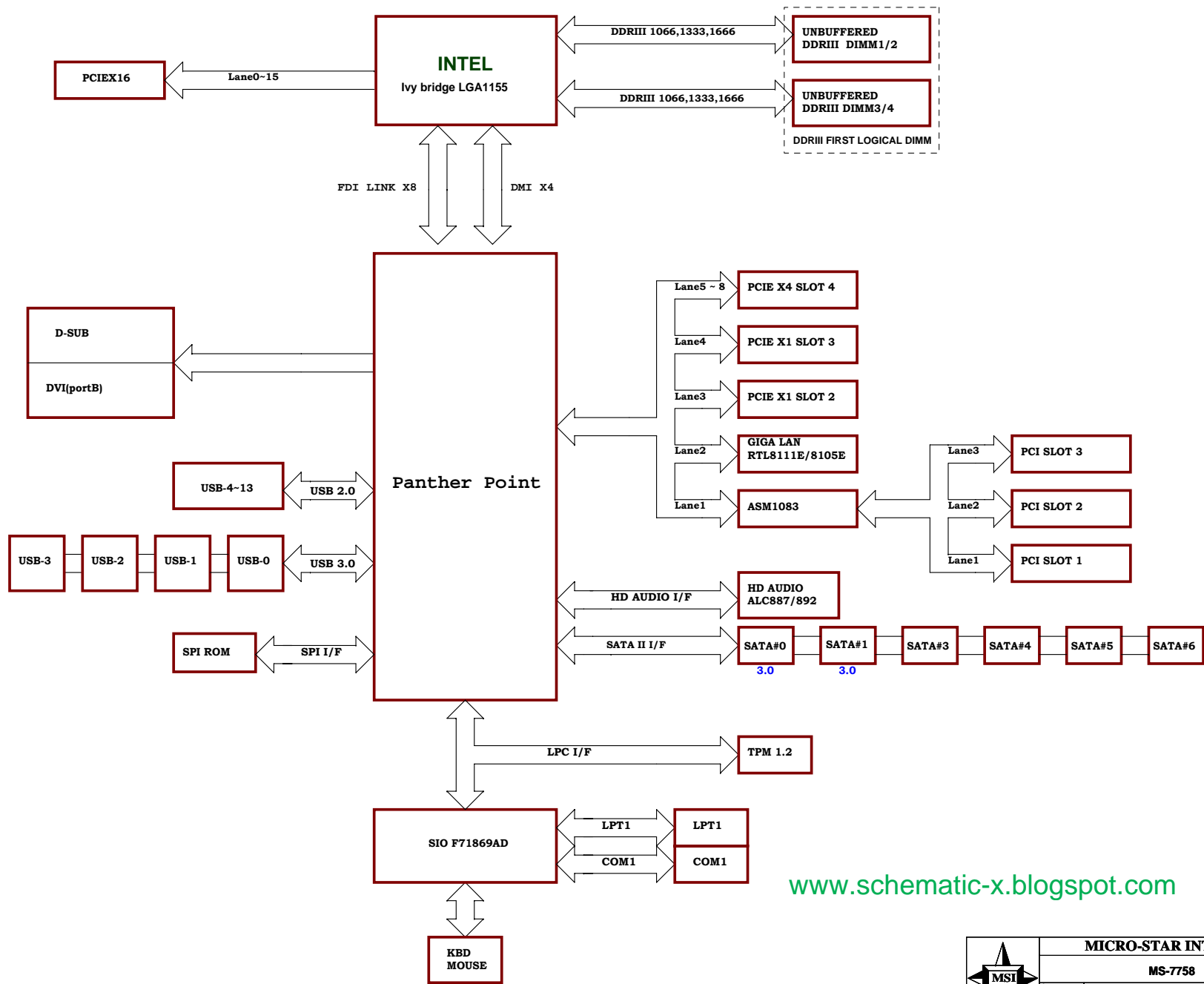
PCI Express (X4) Slot * 1

REAL USB3.0 *2

PCI Slot * 3

FRONT USB3.0 *2

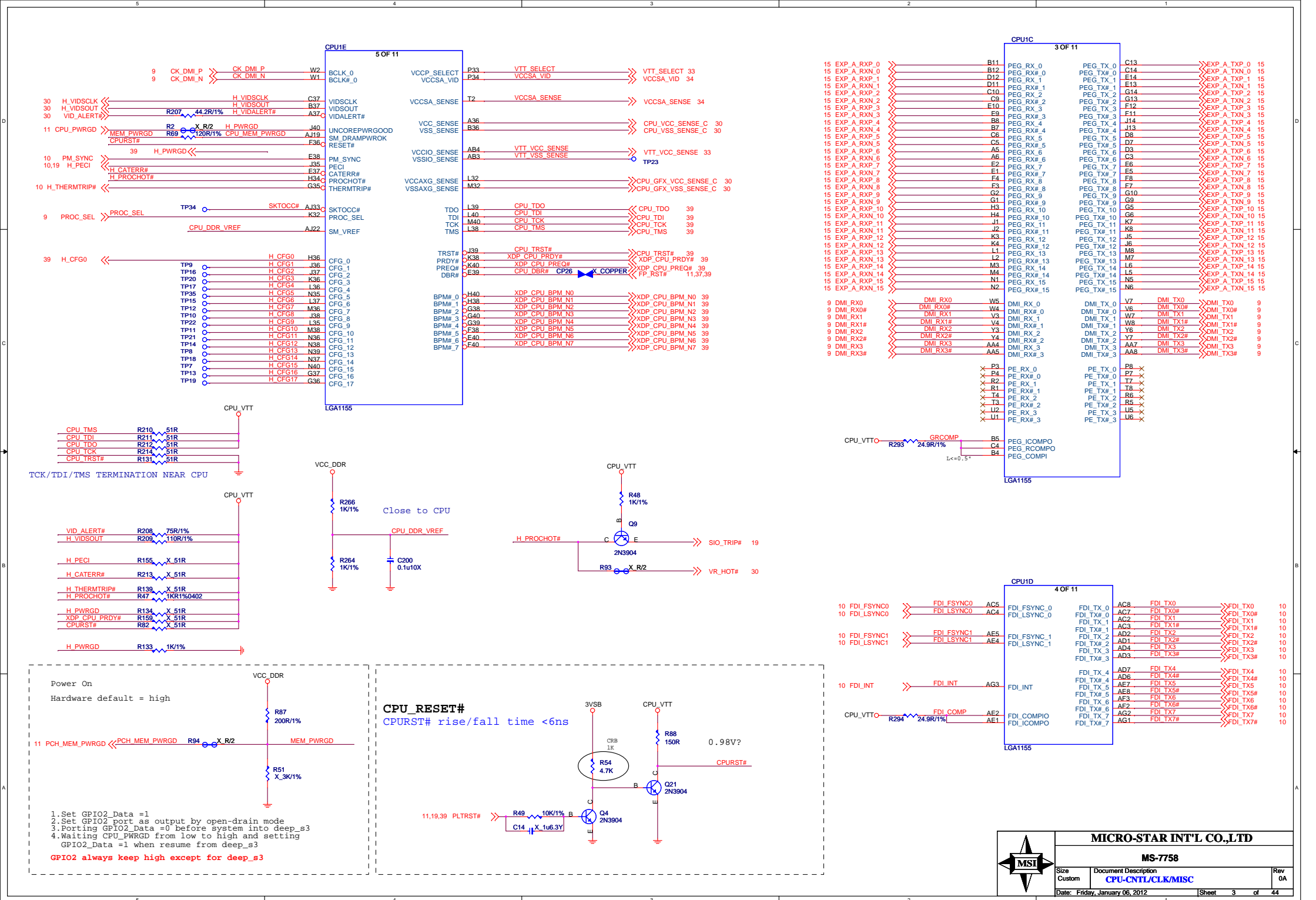
MS-7758 Block Diagram

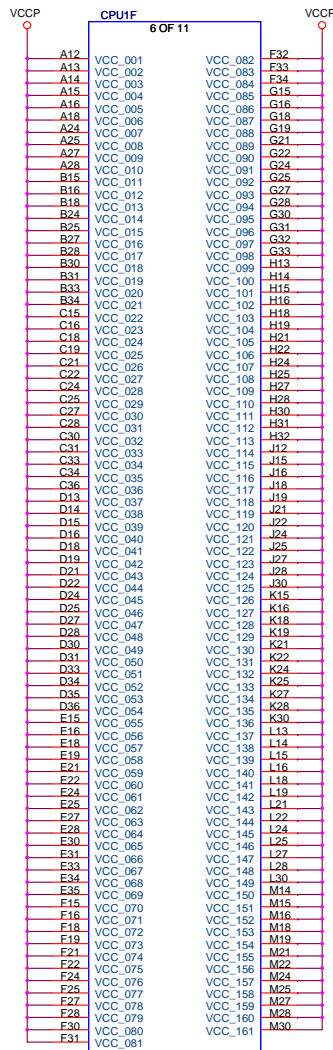


Slot Sequence:

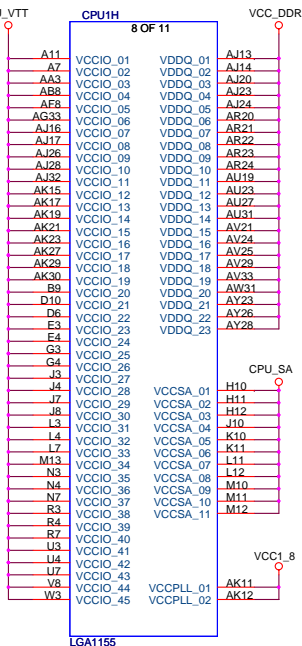
- PCIE X1
- PCIE X16
- PCIE X1
- PCI SLOT
- PCIE X16(X4)
- PCI SLOT
- PCI SLOT

www.schematic-x.blogspot.com





(1.05V / 1.00V)

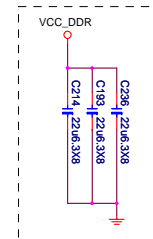


(0.925V / 0.85V)

VCCP: 112A
CPU_VTT: 8.2A
CPU_SA: 8.8A
VCC_DDR: 4.5A
VCC1_8: 1.6A

+1.5V_DDR3-Decoupling

CPU SOCKET CAVITY CAPS



+CPU_SA Decoupling

Backside



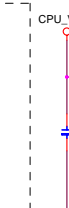
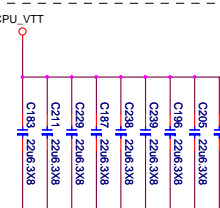
+VCC1_8 Decoupling

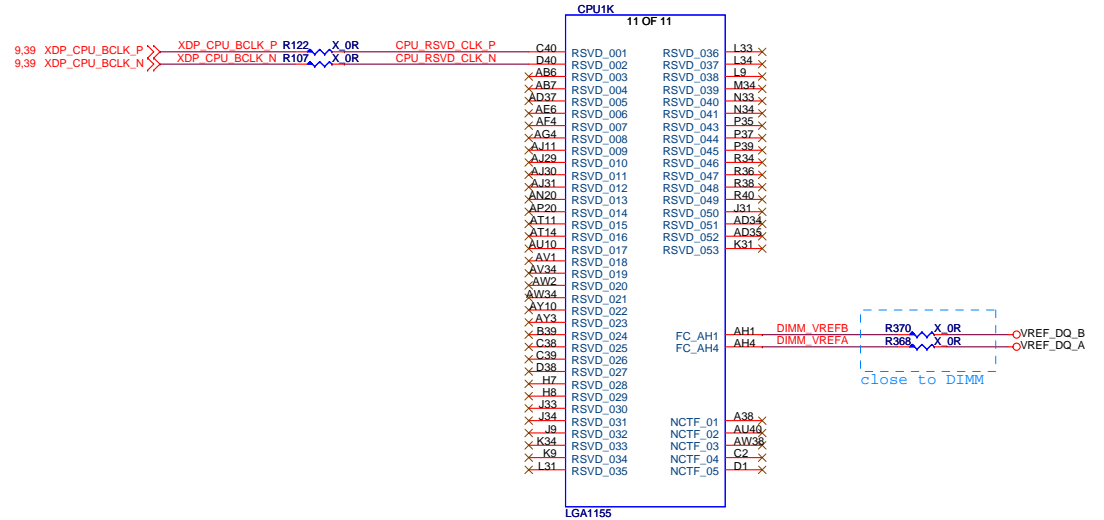
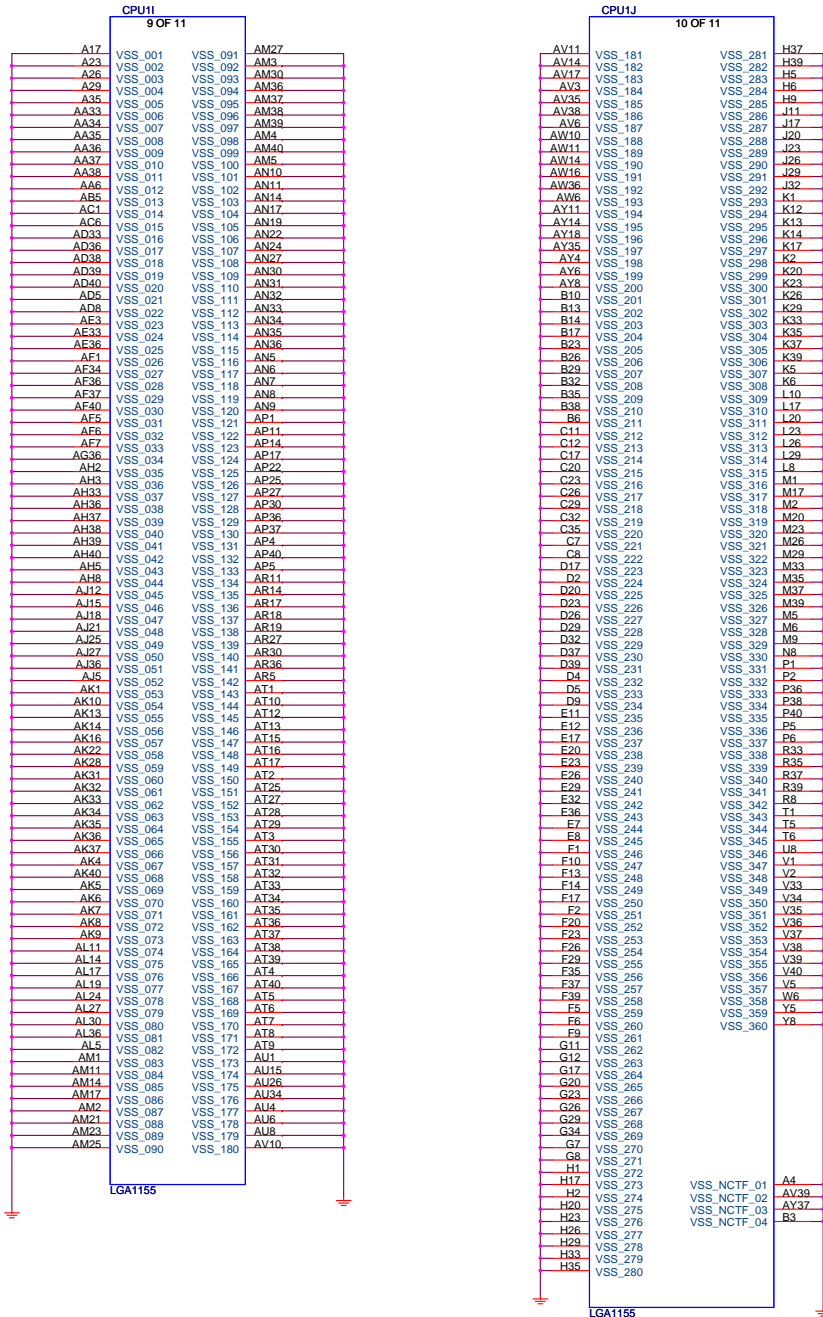
Backside



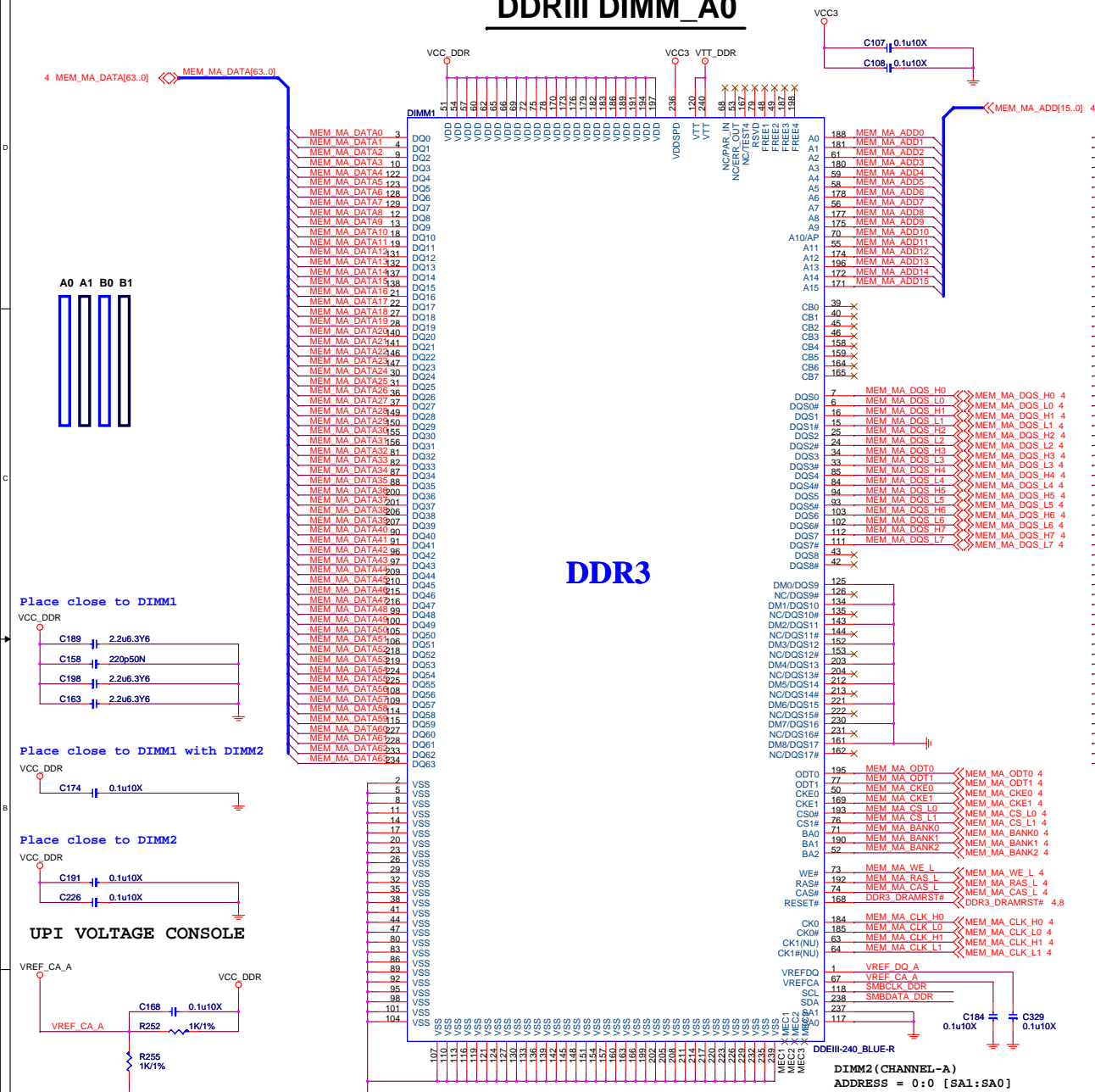
+CPU_VTT Decoupling

CPU SOCKET CAVITY CAPS





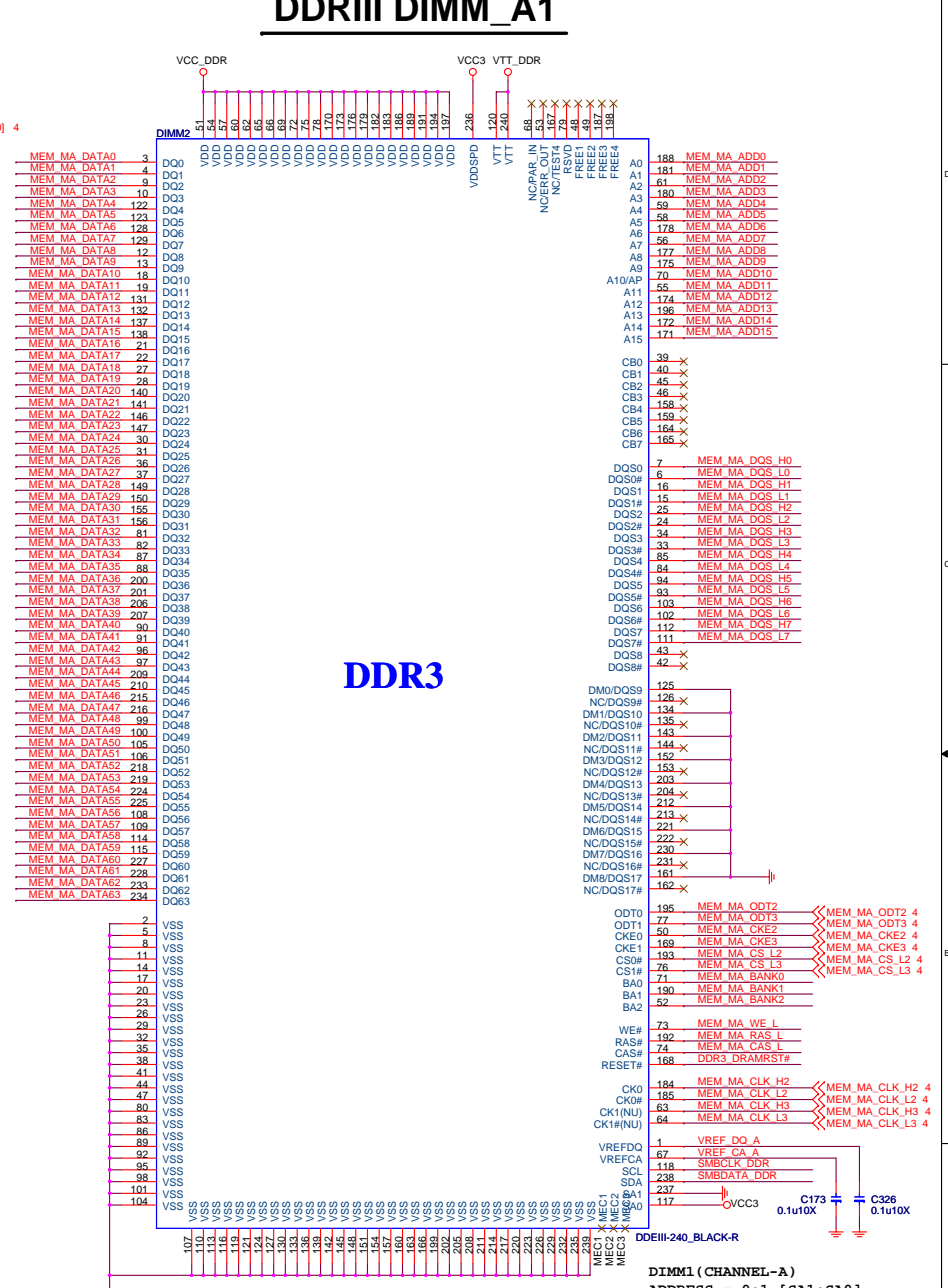
DDRIII DIMM_A0



DDR3

```
DIMM2 ( CHANNEL-A )
ADDRESS = 0:0 [SA1:SA0]
```

DDRIII DIMM_A1



DDR3

DIMM1 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

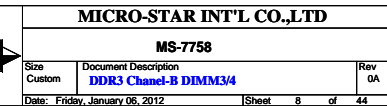
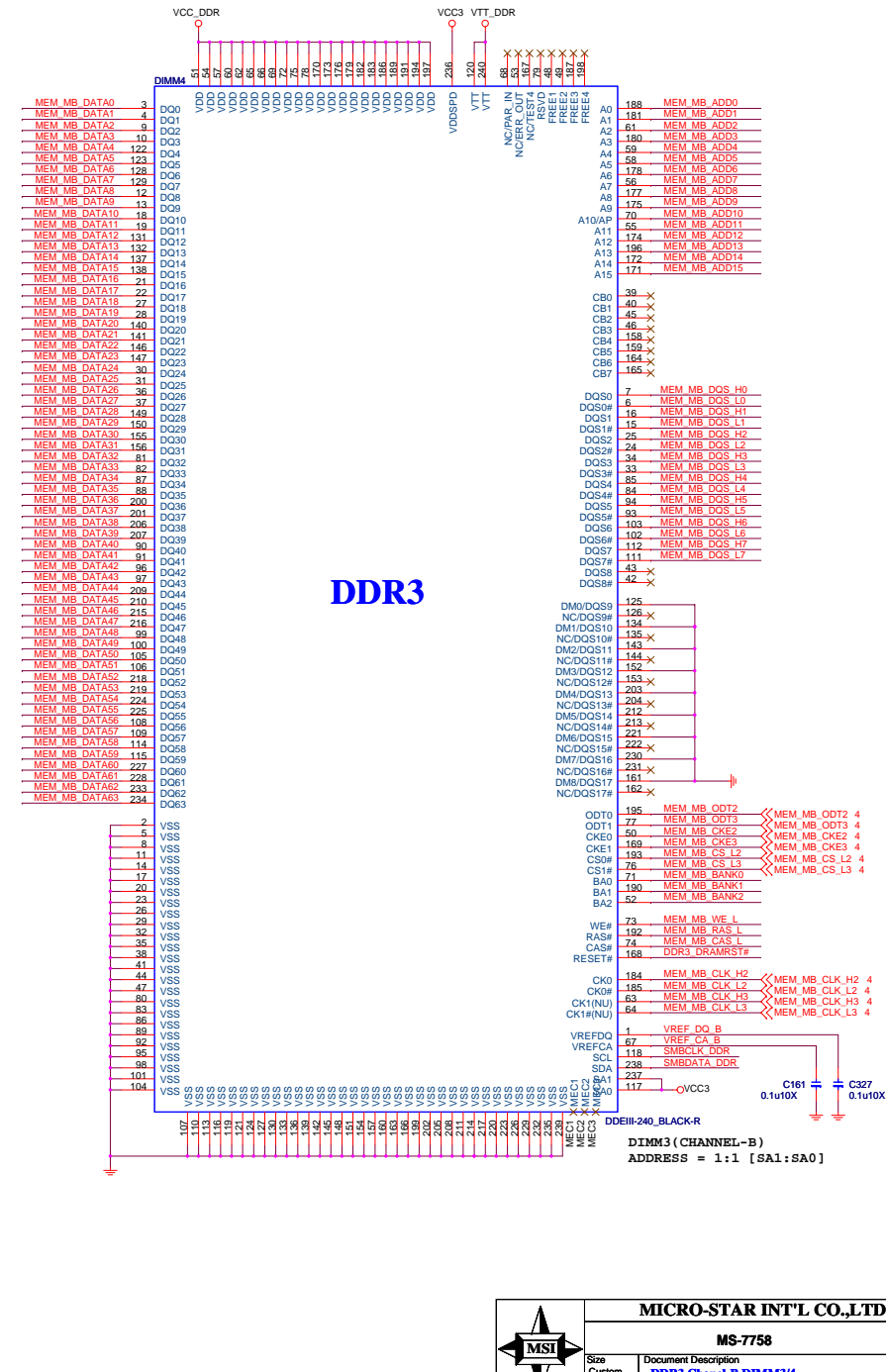


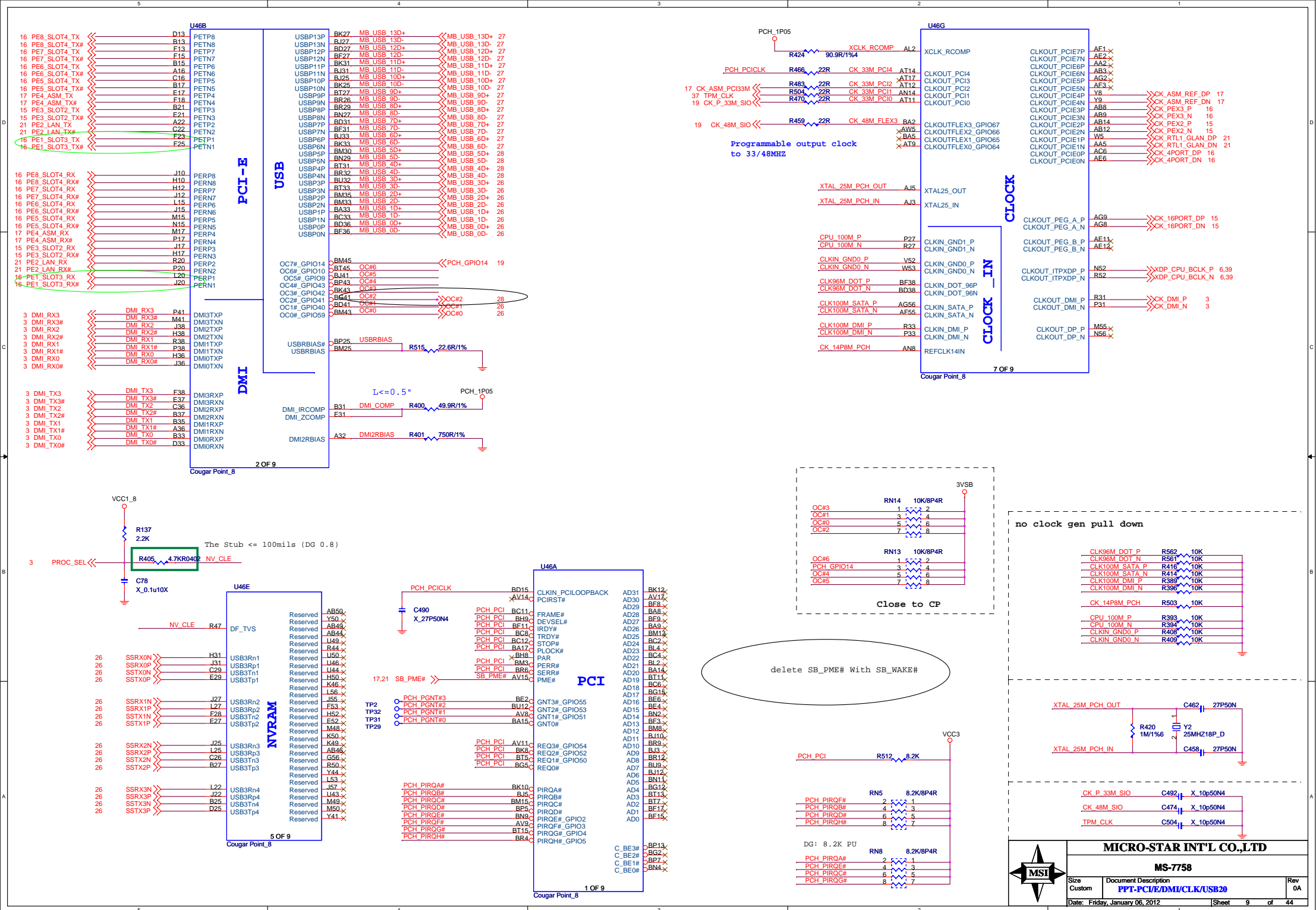
MICRO-STAR INT'L CO.,LTD

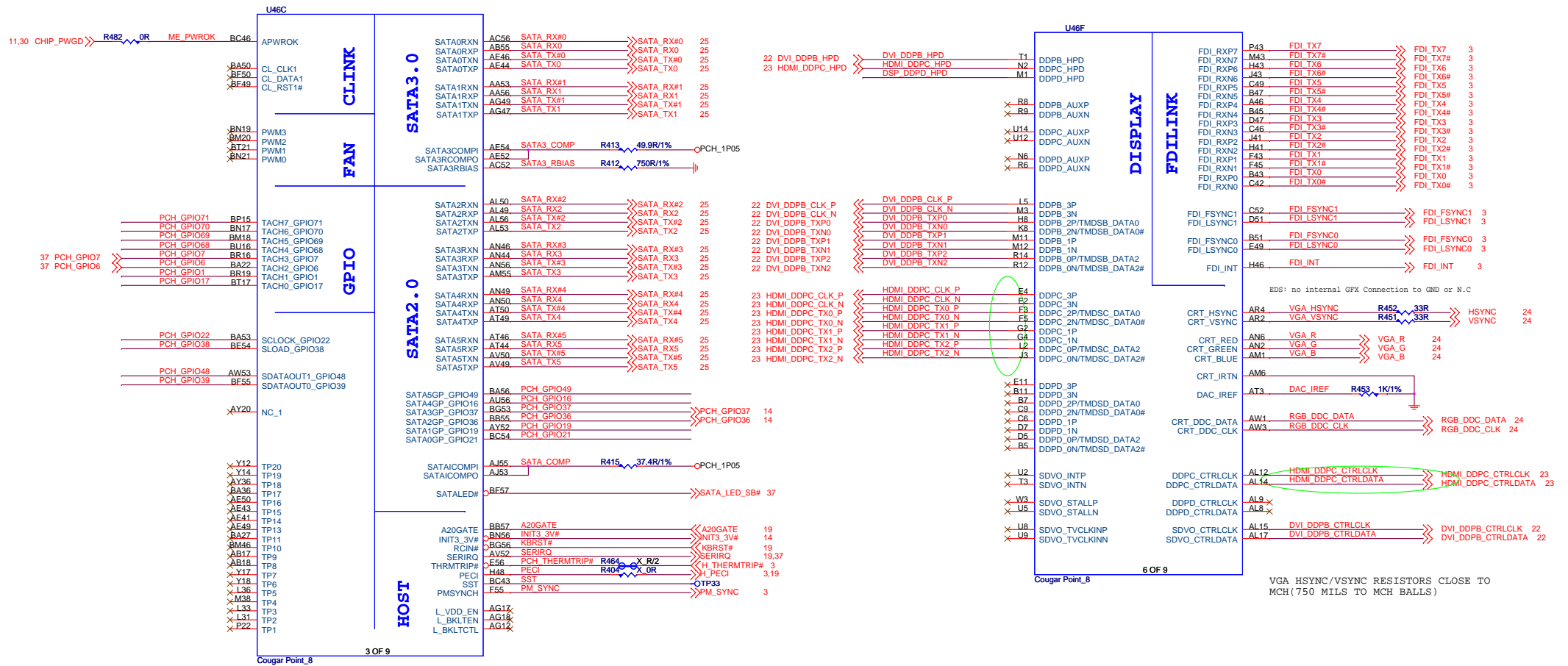
MS-7758

Size Custom	Document Description DDR3 Chane1-A DIMM1/2	Rev 0A
Date: Friday, January 06, 2012		Sheet 7 of 44

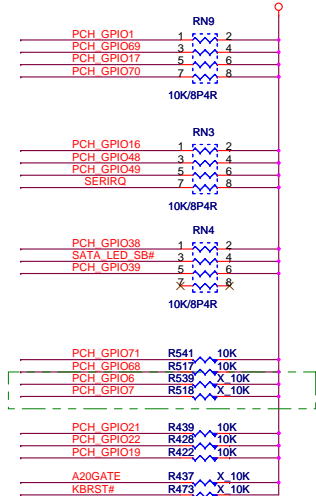
DDRIII DIMM_B1



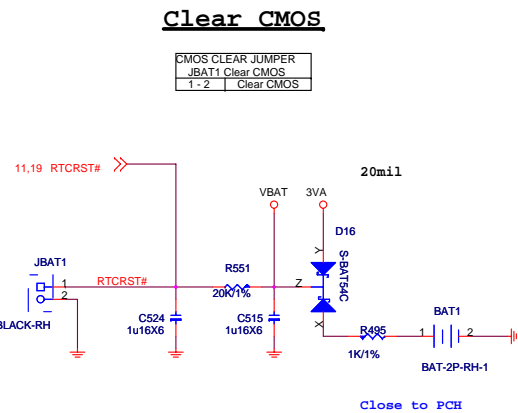




Pull HIGH for PCH



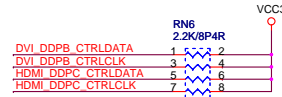
RTC and CLR_CMOS



No Display port(pull down)



Enable VGA(CTRLCLK/DATA Pull High)



Close to PCH within 250 mils.



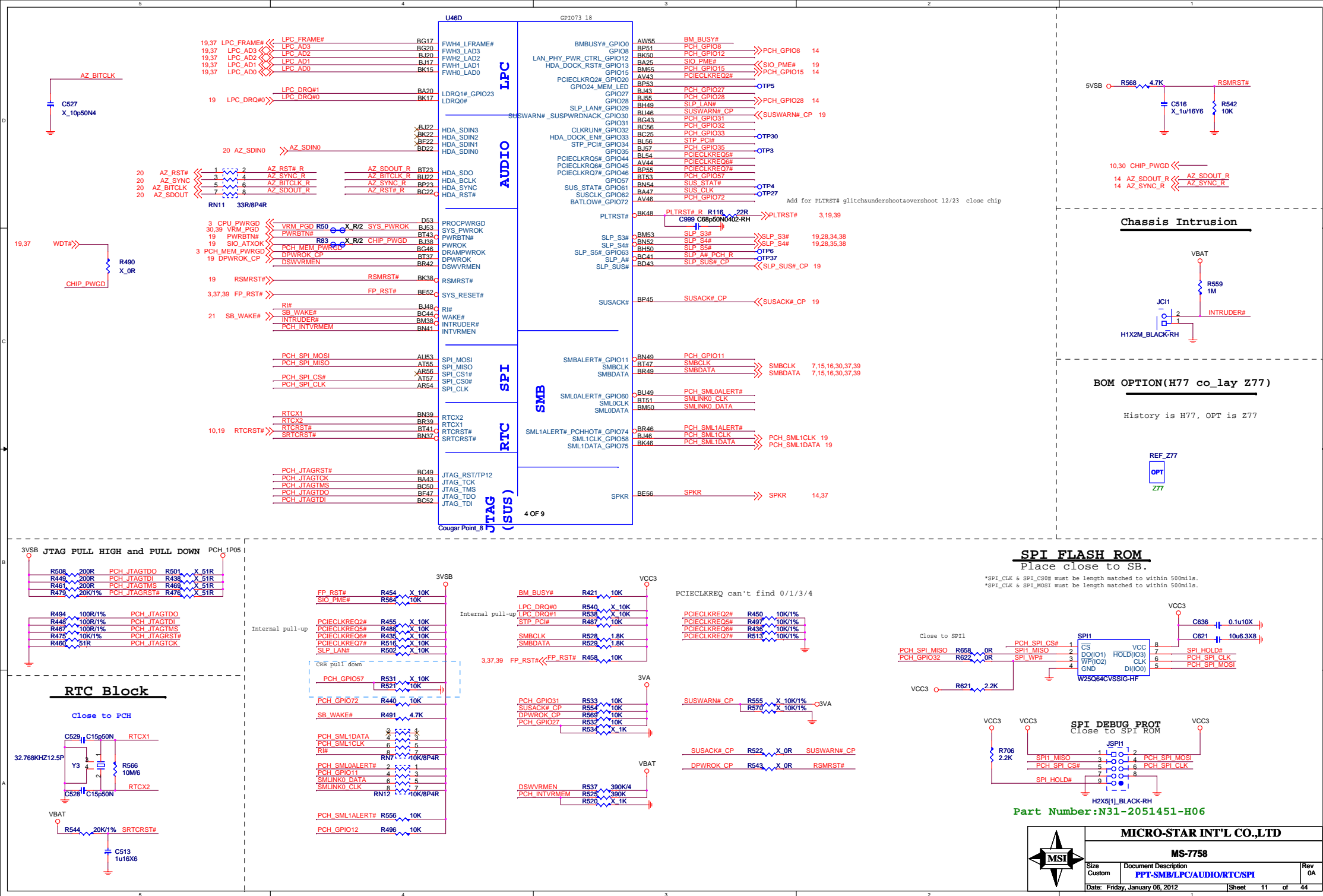
MSI

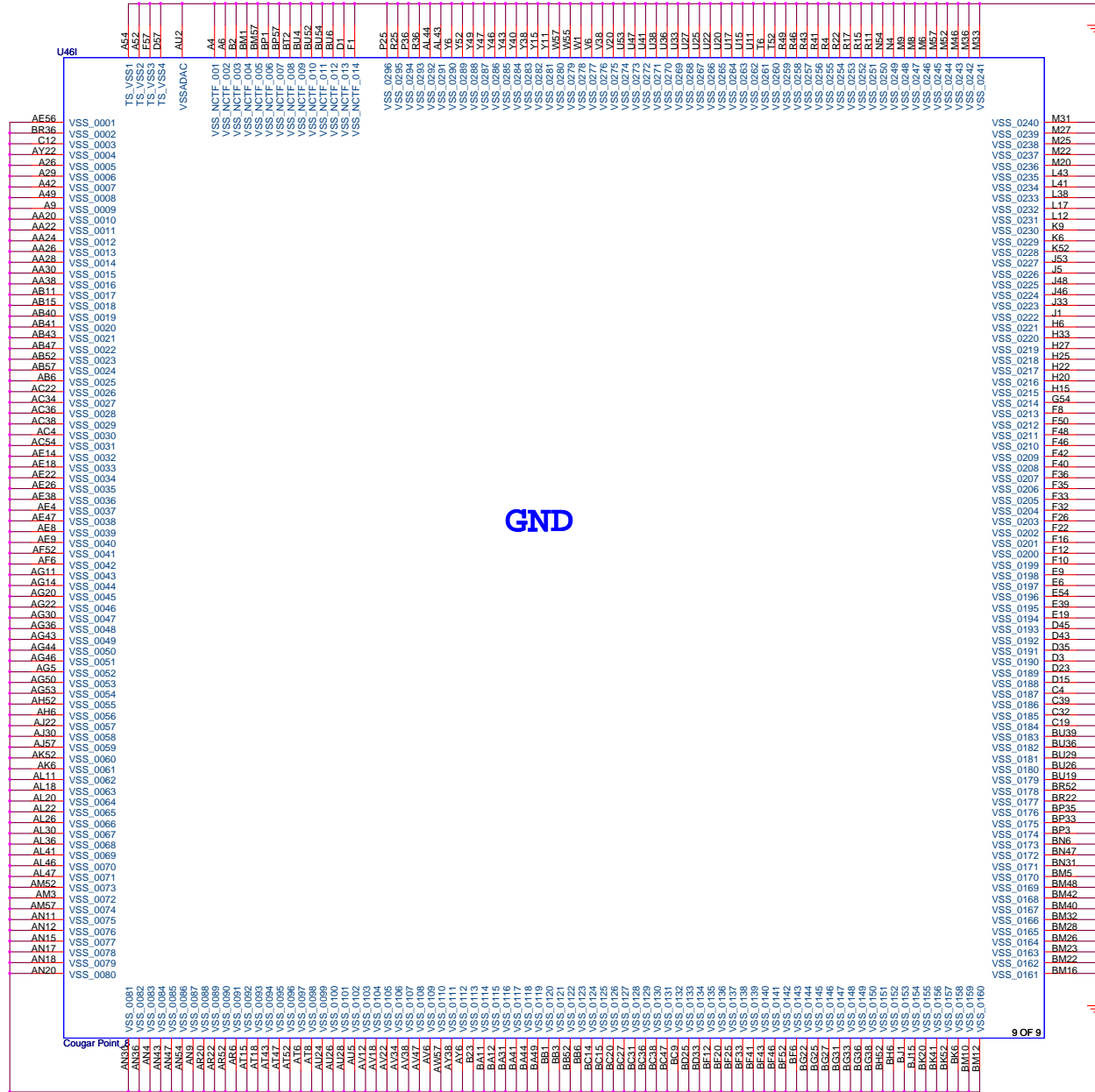
MICRO-STAR INT'L CO.,LTD

MS-7758

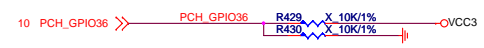
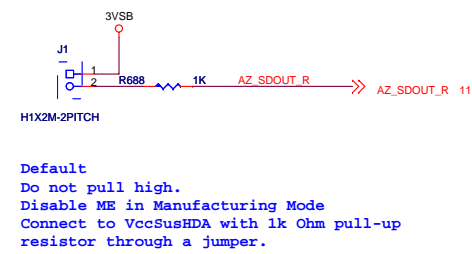
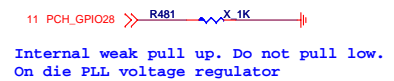
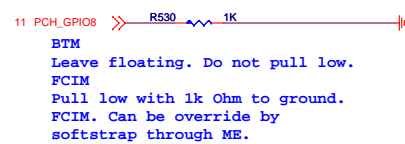
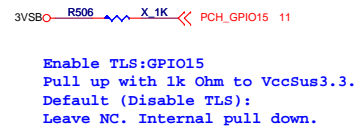
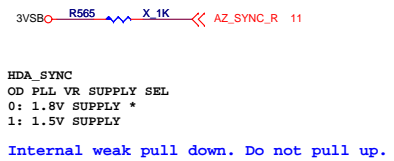
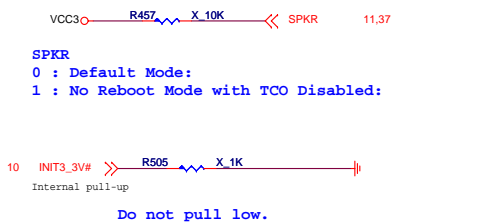
Size Custom Document Description PPT-SATA/HOST/GPIO/VGA/CCMOS Rev 0A

Date: Friday, January 06, 2012 Sheet 10 of 44





PCH Straps



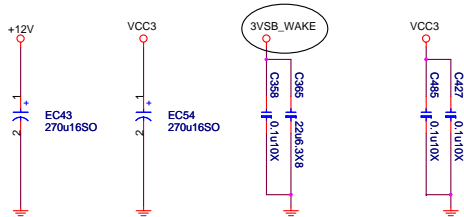
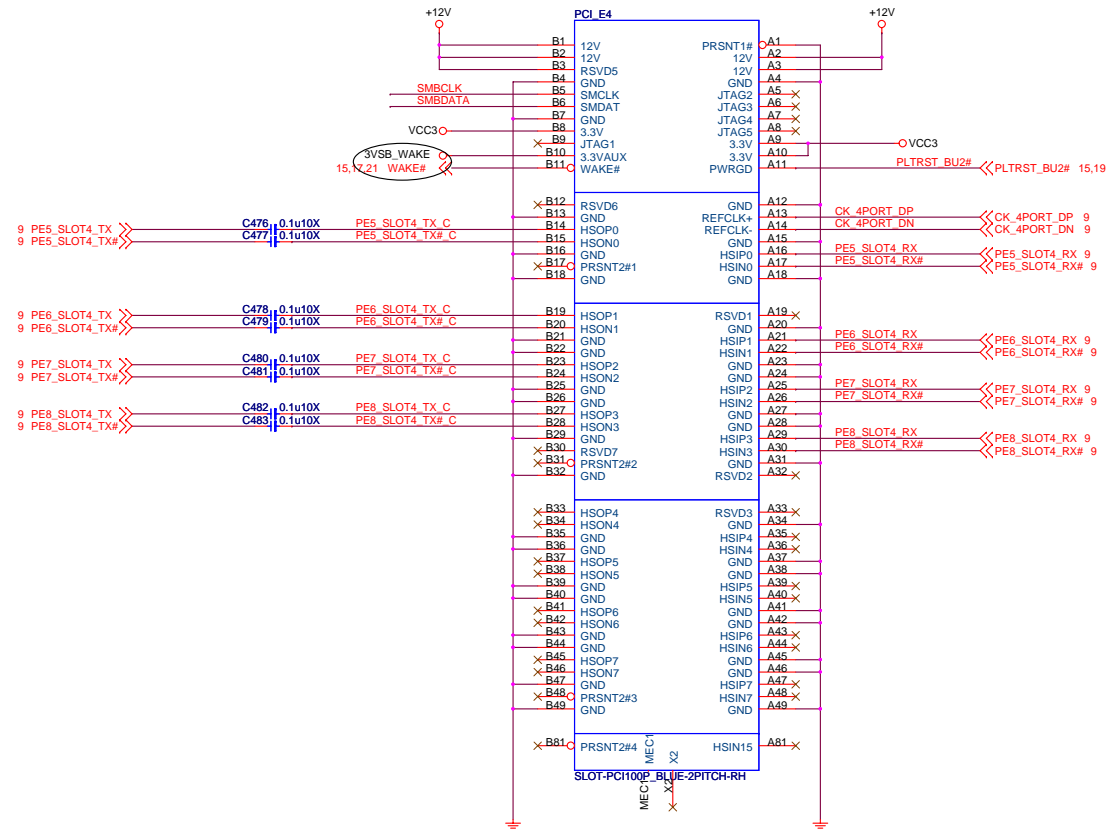
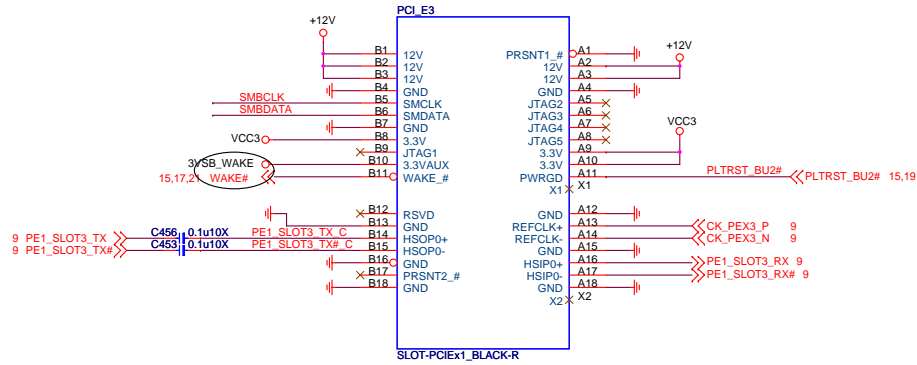
Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

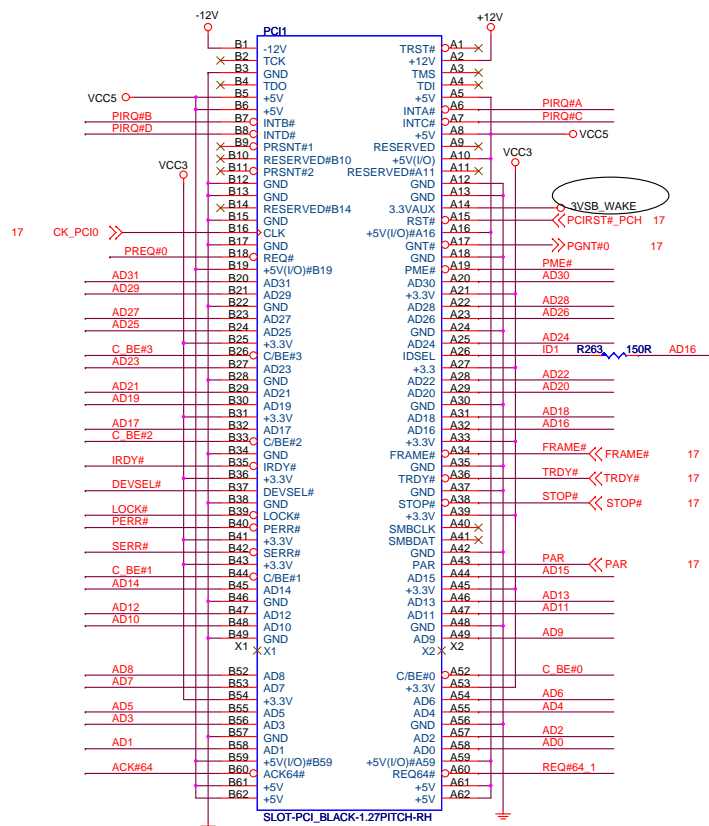


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

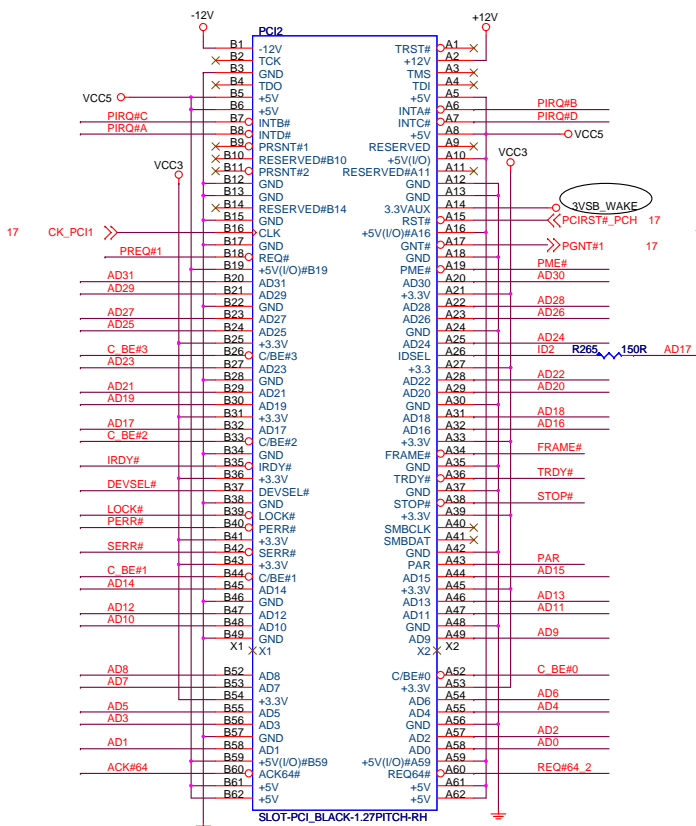
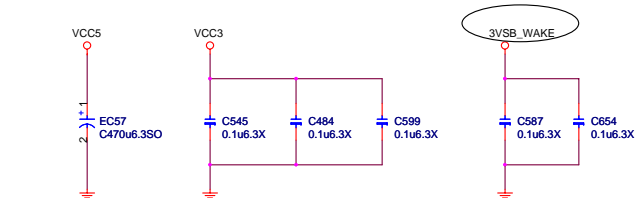
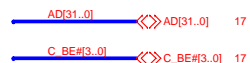
7,11,15,30,37,39 SMBCLK SMBCLK
7,11,15,30,37,39 SMBDATA SMBDATA

PCI Express X4 Slot



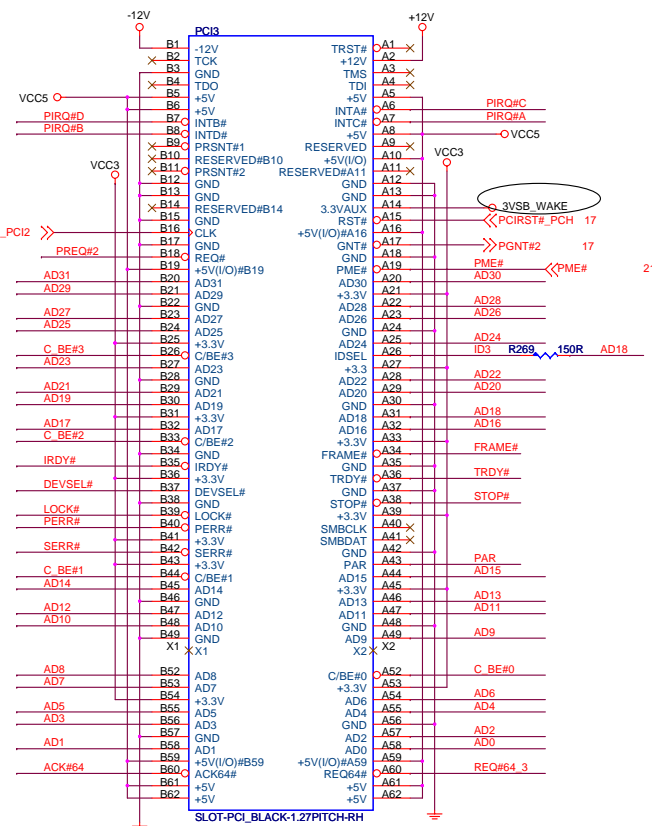
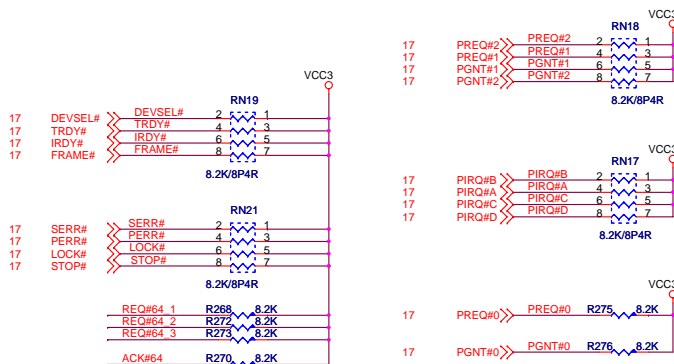


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A



IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS

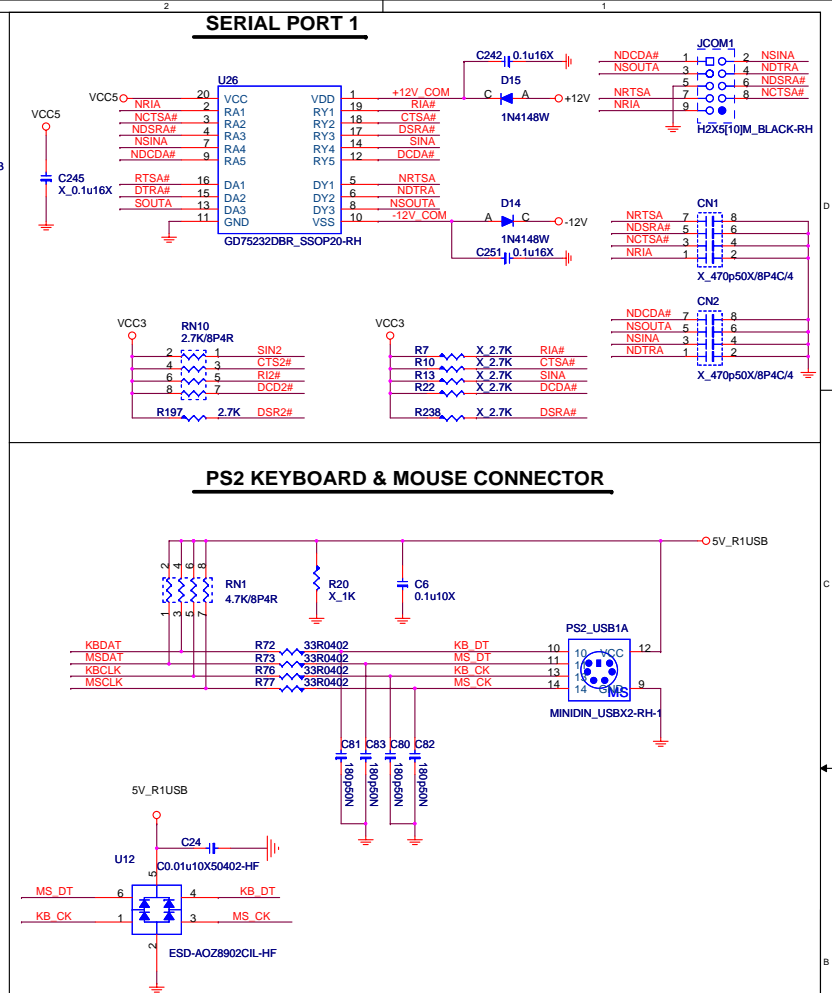


IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

PCI slot (X3)		
+3.3Vaux (wake)	-	1125mA
+3.3Vaux (no wake)	-	60mA
+3.3V	-	7.6A
+5V	-	15A
+12V	-	1.5A

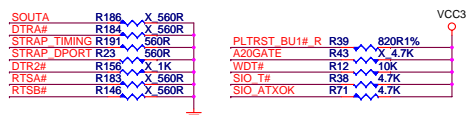


MICRO-STAR INT'L CO.,LTD		
MS-7758		
Size	Document Description	Rev
Custom	PCIx1 Slots	0A
Date: Friday, January 06, 2012	Sheet	18 of 44



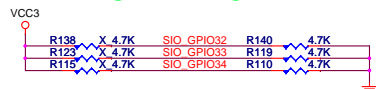
LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Couragar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP SPORT(SOUT2)	Enable 80 Port	Disable 80 Port
RTSA#		



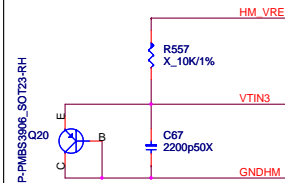
	GPI034	GPI033	GPI032
H77	0	0	0
Z77	0	0	0
Z77_	0	0	1
JUSB CHARGE			

OPT BOM



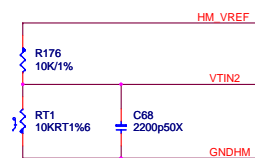
System Thermal

Close to Hot point S/IO

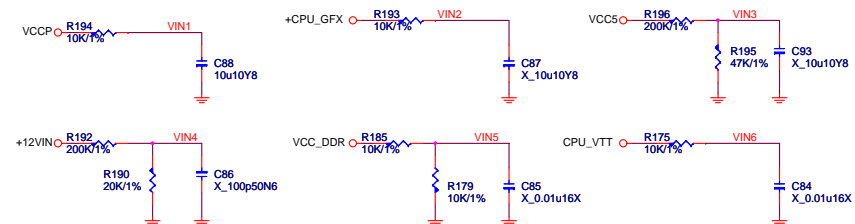


System Thermal

Close to Hot point MOS Q79



HW Monitor - Voltage

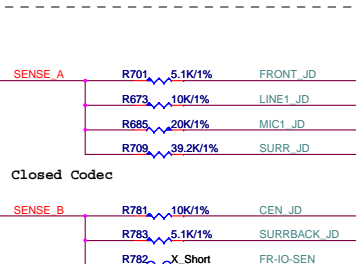


MICRO-STAR INT'L CO.,LTD

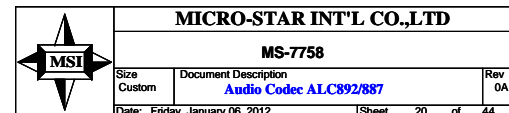
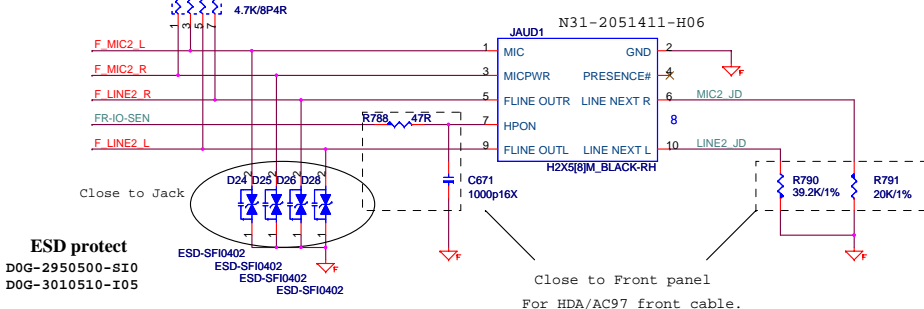
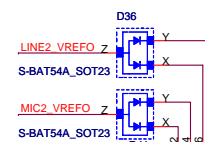
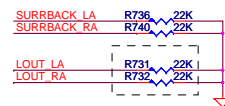
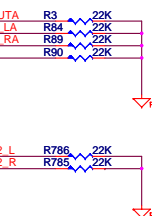
MS-7758

Size Custom	Document Description SIO-Fintek F71869AD	Rev 0A
----------------	--	-----------

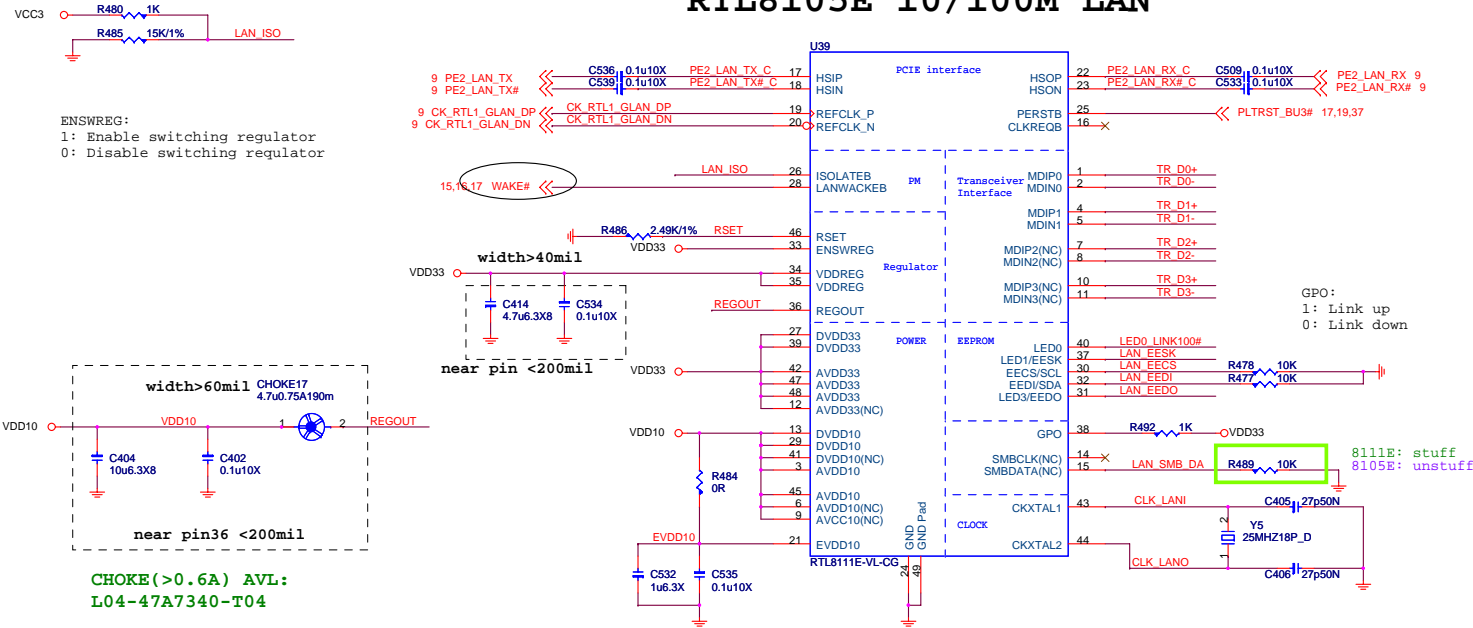
ALC892



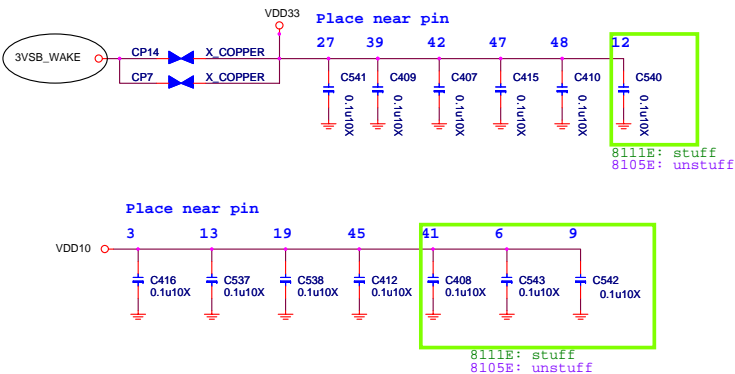
SPDIF OUT




```
RTL8111E Giga LAN
RTL8105E 10/100M LAN
```



3.3v Power on rise time : 1~100ms. MAX: 163mA

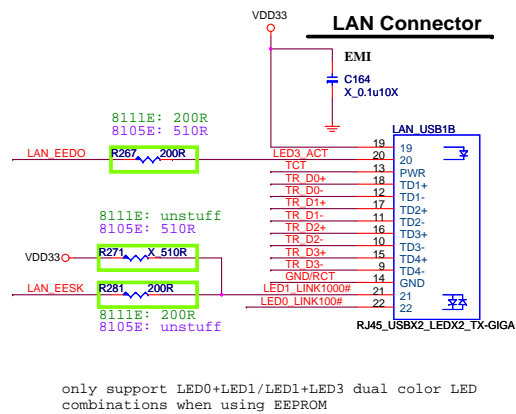


8111E POWER Consumption

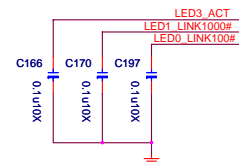
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

8105E POWER Consumption

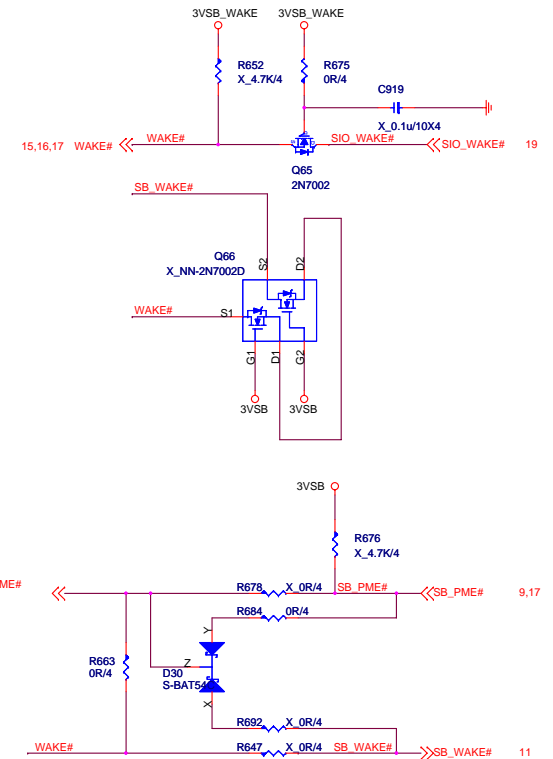
	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11











only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM



LAN/PCIE/PCI Wake Up CTRL Circuit



Giga-Lan	10/100-Lan
N58-22F0731 Link Yellow Active Blinking 1000 Orange 100 Green 10 None	N58-22F0771 Link Yellow Active Blinking 100 Green 10 None
19  20  Yellow	19  20  Yellow
Orange 21  22  Green	21  22  Green

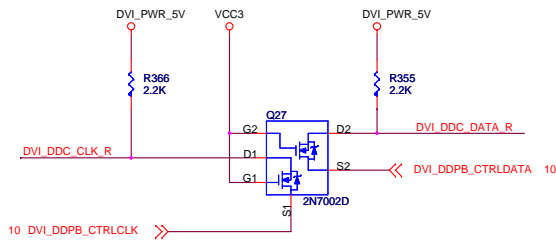
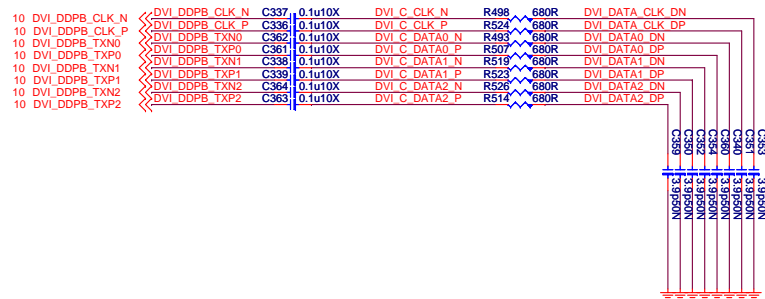


MICRO-STAR INT'L CO.,LTD

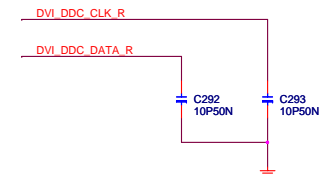
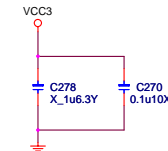
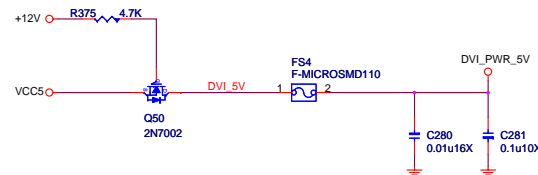
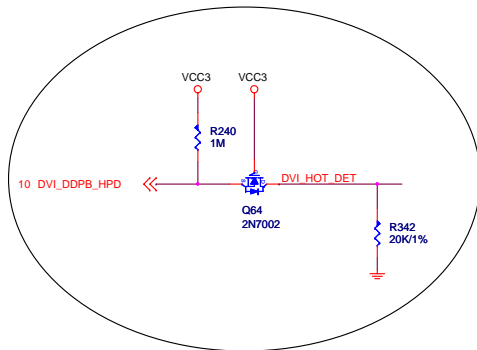
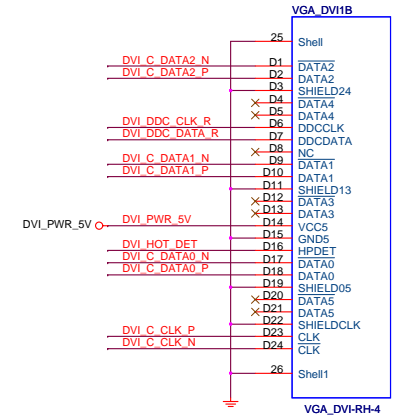
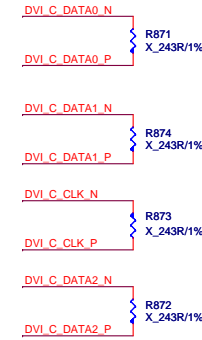
MS-7758

Size Custom	Document Description LAN-RTL8111E/8105E	Rev 0A
Date: Friday, January 06, 2012	Sheet 21 of 44	

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

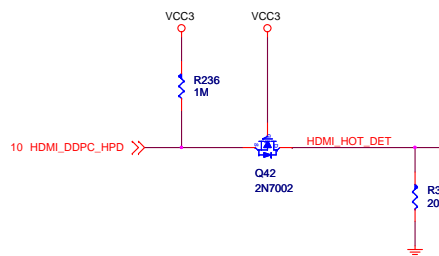
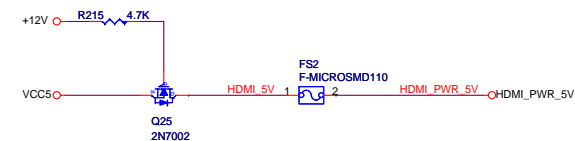
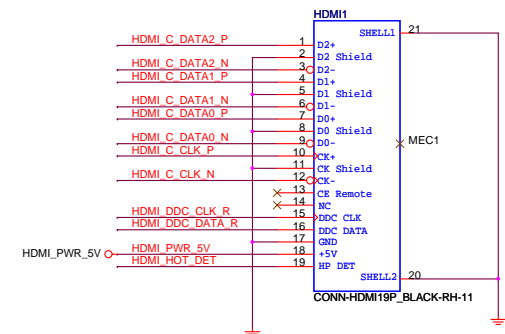
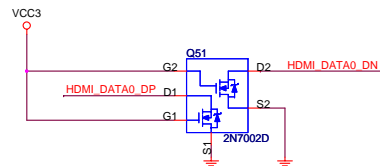
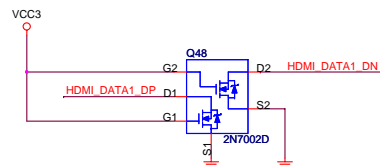
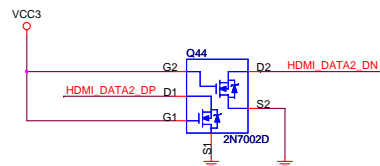
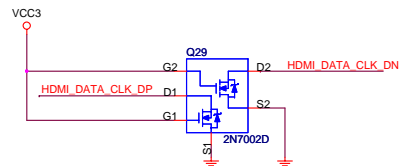
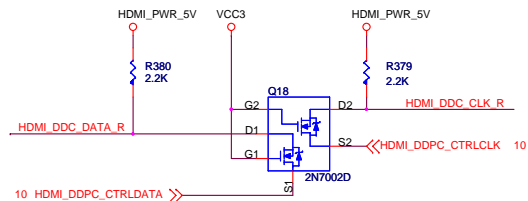


For EMI



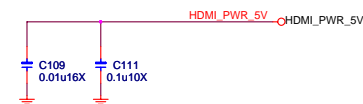
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

10 HDMI_DDPC_CLK_P	HDMI_DDPC_CLK_P	C140	0.1u10X	HDMI_C_CLK_P	R545	680R	HDMI_DATA_CLK_DP
10 HDMI_DDPC_CLK_N	HDMI_DDPC_CLK_N	C142	0.1u10X	HDMI_C_CLK_N	R553	680R	HDMI_DATA_CLK_DN
10 HDMI_DDPC_TX2_P	HDMI_DDPC_TX2_P	C134	0.1u10X	HDMI_C_DATA2_P	R527	680R	HDMI_DATA2_DP
10 HDMI_DDPC_TX2_N	HDMI_DDPC_TX2_N	C132	0.1u10X	HDMI_C_DATA2_N	R547	680R	HDMI_DATA2_DN
10 HDMI_DDPC_TX1_P	HDMI_DDPC_TX1_P	C136	0.1u10X	HDMI_C_DATA1_P	R548	680R	HDMI_DATA1_DP
10 HDMI_DDPC_TX1_N	HDMI_DDPC_TX1_N	C138	0.1u10X	HDMI_C_DATA1_N	R549	680R	HDMI_DATA1_DN
10 HDMI_DDPC_TX0_P	HDMI_DDPC_TX0_P	C124	0.1u10X	HDMI_C_DATA0_P	R552	680R	HDMI_DATA0_DP
10 HDMI_DDPC_TX0_N	HDMI_DDPC_TX0_N	C121	0.1u10X	HDMI_C_DATA0_N	R546	680R	HDMI_DATA0_DN



For EMI

HDMI_C_CLK_N	R235	X_180R/1%
HDMI_C_CLK_P	R235	X_180R/1%
HDMI_C_DATA0_N	R225	X_180R/1%
HDMI_C_DATA0_P	R225	X_180R/1%
HDMI_C_DATA1_N	R233	X_180R/1%
HDMI_C_DATA1_P	R233	X_180R/1%
HDMI_C_DATA2_N	R231	X_180R/1%
HDMI_C_DATA2_P	R231	X_180R/1%



EMI

HDMI_DDC_CLK_R	C572	X 0.1u16X
HDMI_DDC_DATA_R	C571	X 0.1u16X
HDMI_HOT_DET	C570	X 0.1u16X



MICRO-STAR INT'L CO.,LTD

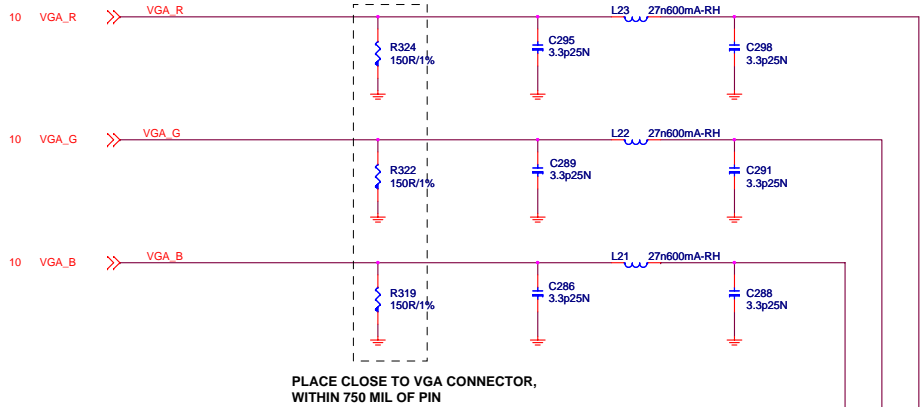
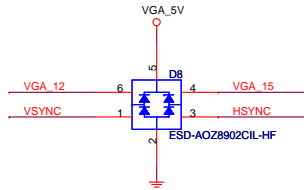
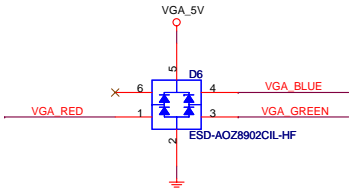
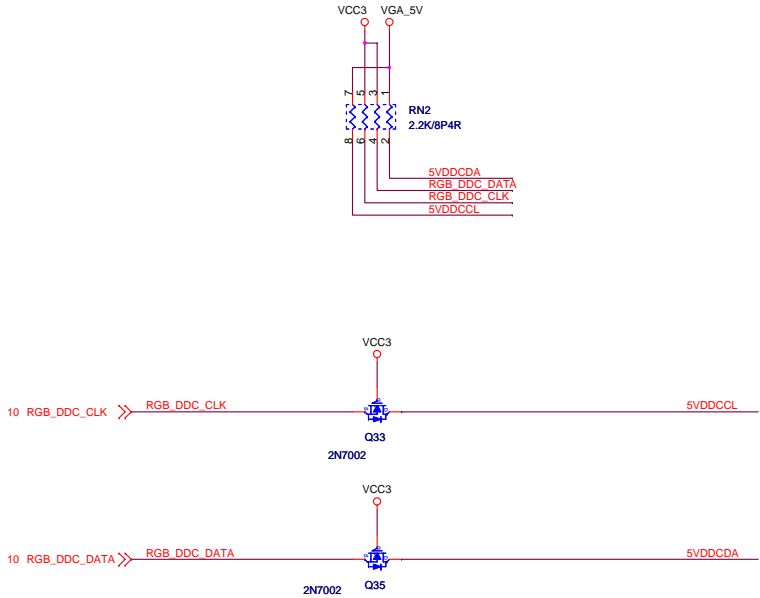
MS-7758

Size	Document Description	Rev
Custom	HDMI Connector	0A
Date: Friday, January 06, 2012	Sheet 23 of 44	

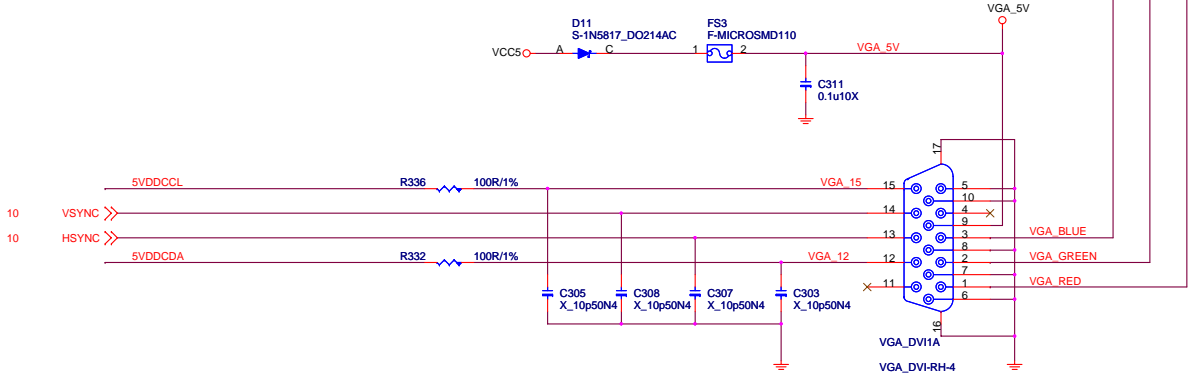
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Levelshift

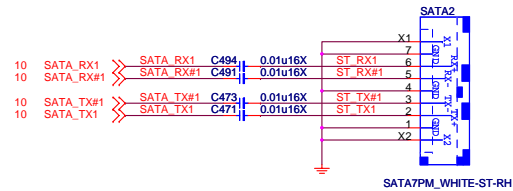
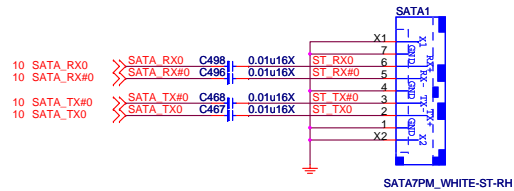


PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN

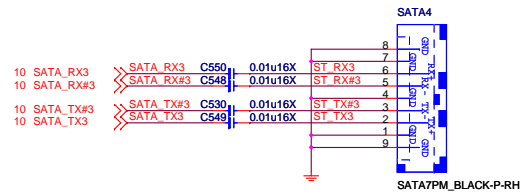
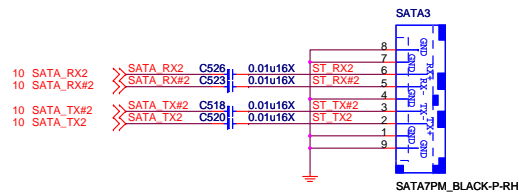


SATA 6G PORT 0,1

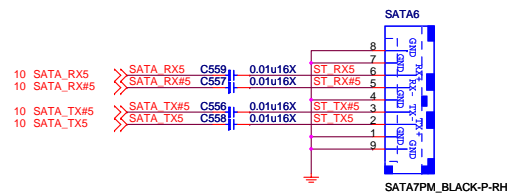
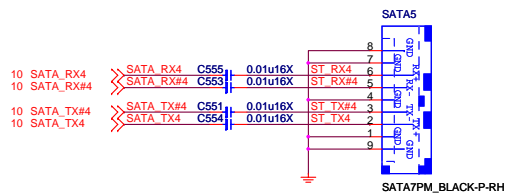
3.0 white



SATA 3G PORT 2,3



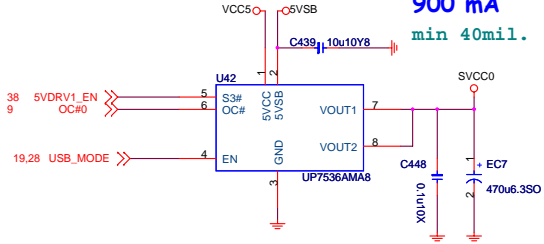
SATA 3G PORT 4,5



FRONT USB30 PORT 0,1

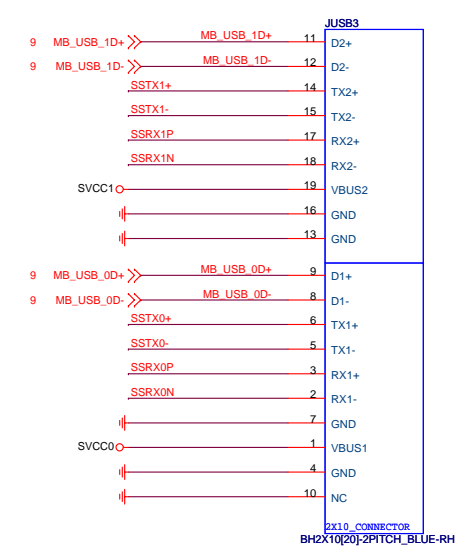
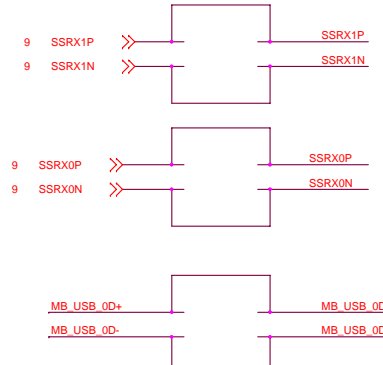
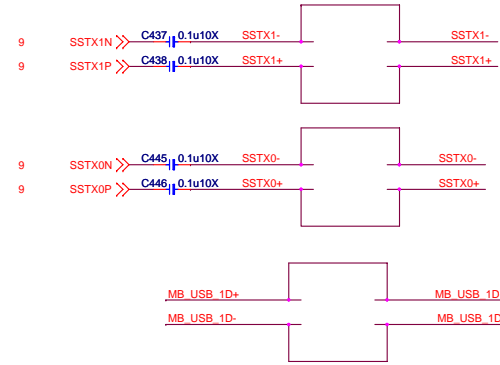
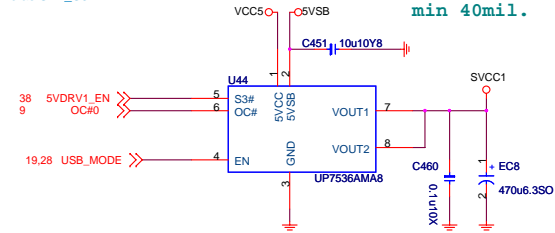
Same as SLP_S3#

900 mA
min 40mil.



Same as SLP_S3#

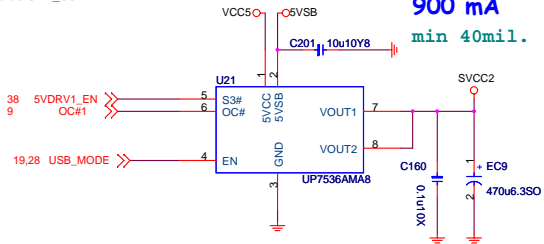
900 mA
min 40mil.



REAR USB30 PORT 2,3

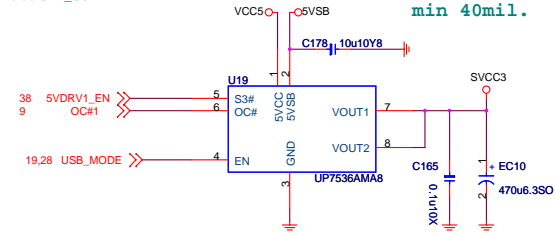
Same as SLP_S3#

900 mA
min 40mil.



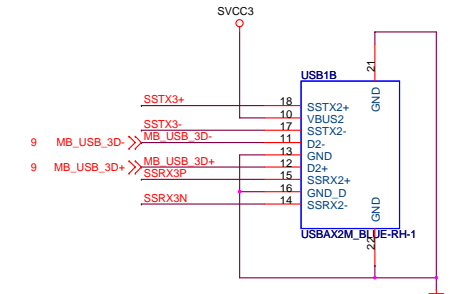
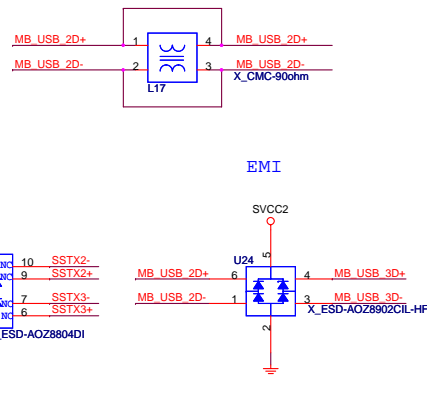
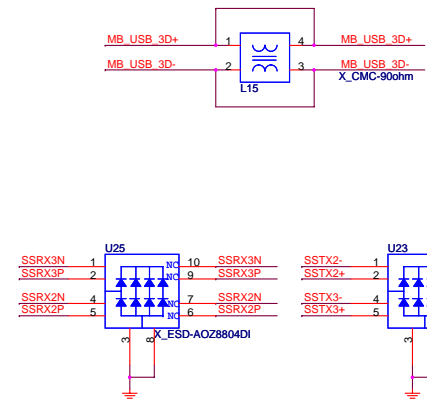
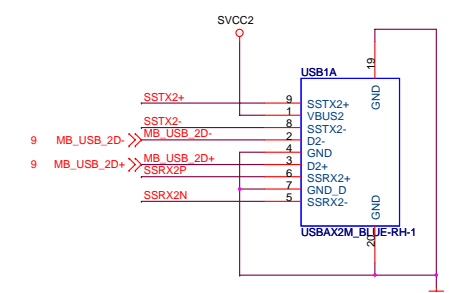
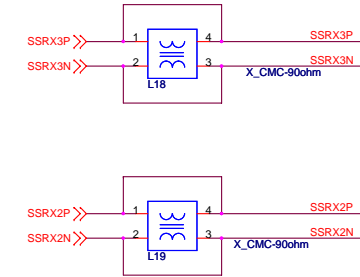
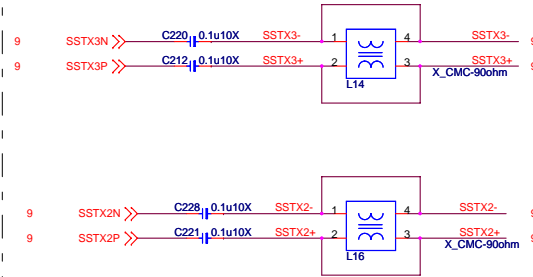
Same as SLP_S3#

900 mA
min 40mil.



USB_MODE
Hi by BIOS programming,
default h/w PD for avoid UP7536 Enable pin floating

USB_MODE States				
MODE	G3	S4/S5	S0	S3
EUP Disable	0	0	1	1
EUP Enable	0	0	1	1



MICRO-STAR INT'L CO.,LTD

MS-7758

Size	Document Description	Rev
Custom	USB3.0 Connector	0A
Date: Friday, January 06, 2012	Sheet 26 of 44	

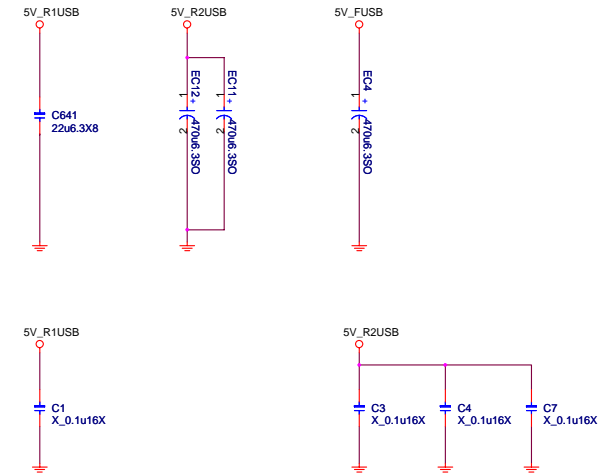
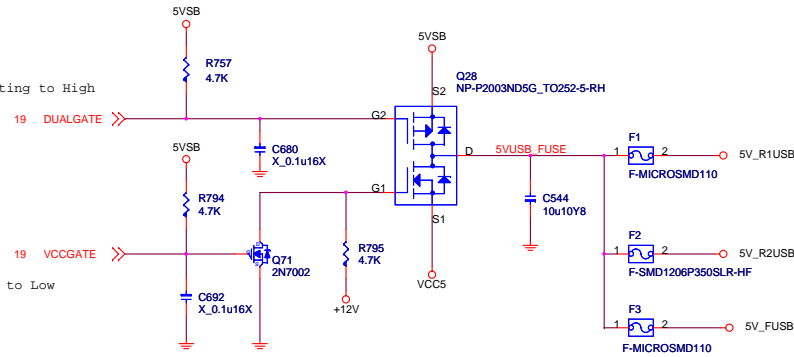
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	1	1	1
S0P5_Gate#	1	1	0

When PS2 in S5 not support wake , S3P5_Gate# in S5 must setting to High

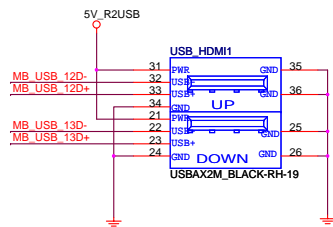
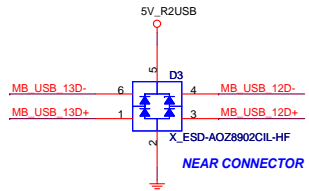
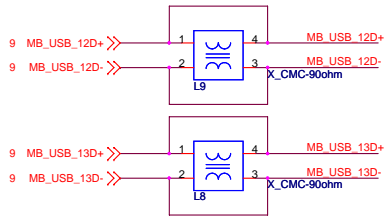
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	0	1	1
S0P5_Gate#	1	1	0

*In S5# (S3P5_Gate # pin status is Tri-state, and can be programmed Low level.

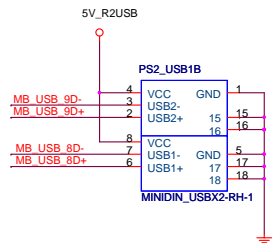
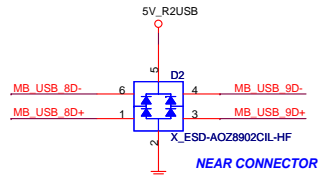
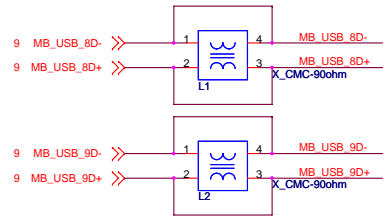
*S3P5_Gate# and S0P5_Gate# can't setting to low together, avoid leakage voltage issue



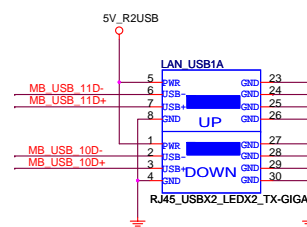
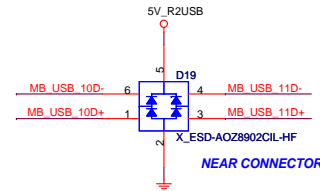
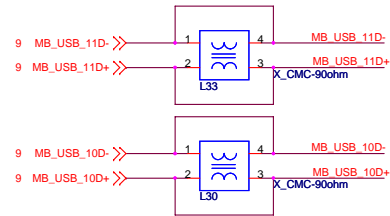
REAR USB PORT 12,13 (With LAN)



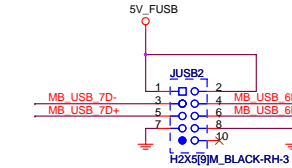
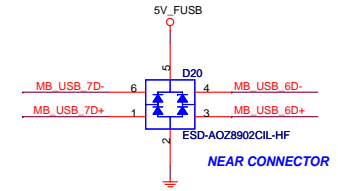
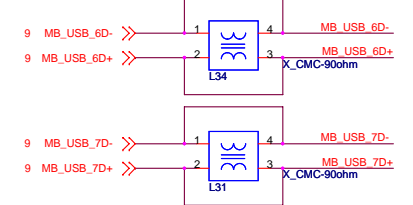
REAR USB PORT 8,9 (With HDMI)



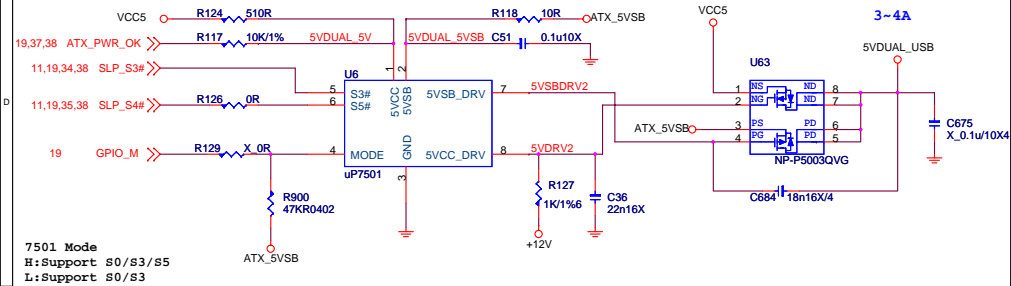
FRONT USB PORT 10,11(With PS2)



FRONT USB PORT 6,7



5VDUAL_USB



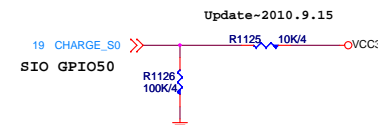
SIO GPIO40 Pin7 (I_VSB3V)

USB_CHARGE: (OD)

0: Don't support USB charge and resume.
1: Support USB charge and resume.

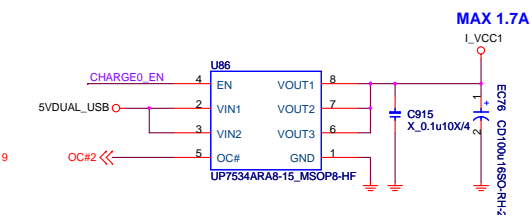
Power plug in , H/W default support USB charge.

Pin power I_3VSB or VBAT
Register power I_3VSB or
VBAT
Register reset I_3VSB or
VBAT



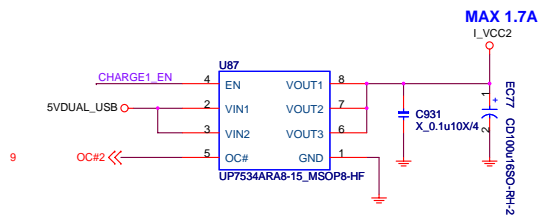
Update-2010.9.15

USB POWER PORT 0 For USB Charging

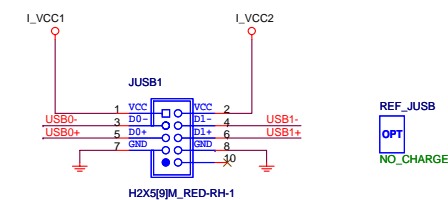
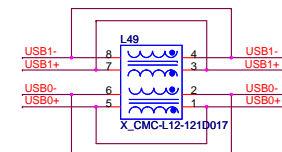


** If your spec will not need bom option, please don't co-lay blue labels.

USB POWER PORT 1 For USB Charging



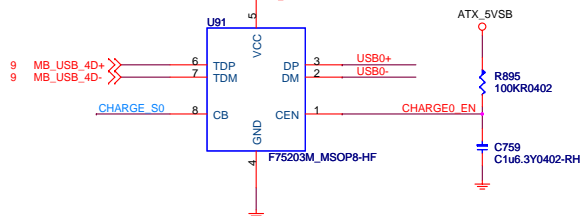
FRONT USB PORT 0,1



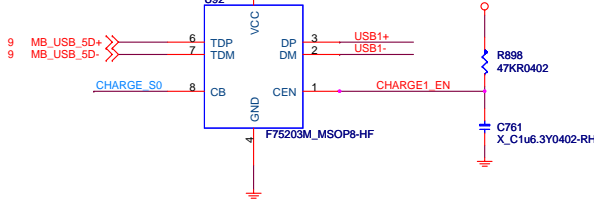
Please name the pin header JUSB1 and use SB USB0,1 link for charger port.

PI5USB14550 has internal EDS diode.

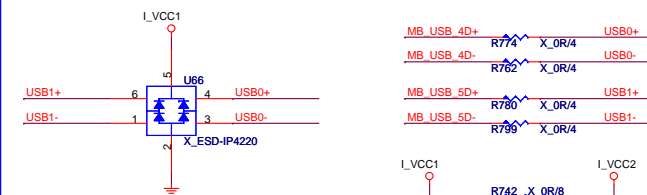
From SB To Pin Header



From SB To Pin Header



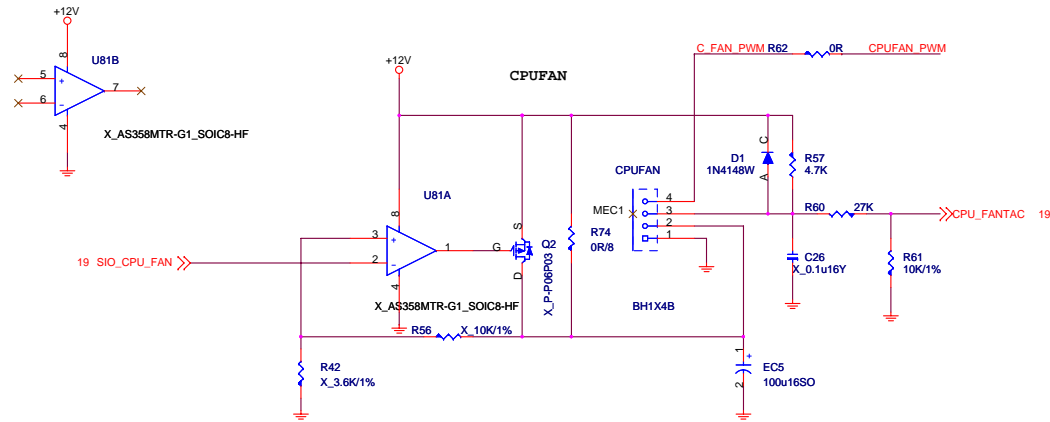
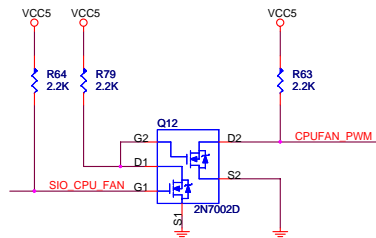
COLAY remove USB charger ic



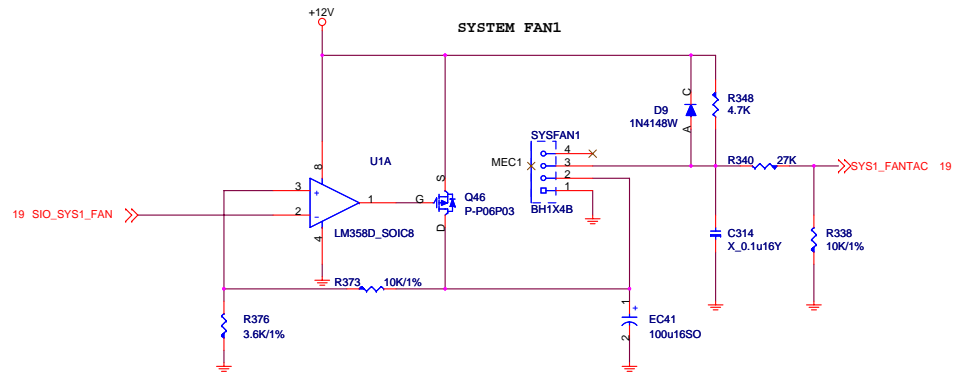
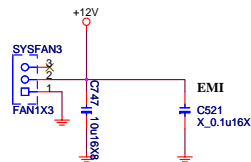
A type
2.70V< D+ <3.1 V
1.85V< D- < 2.1V
For i-Pad / i-Phone 4G charges current up to 1.6A.

Title		
USB FULL CHARGE		
Size	Document Number	Rev
Custom	M45-7758	0A
Date:	Friday, January 06, 2012	Sheet 28 of 44

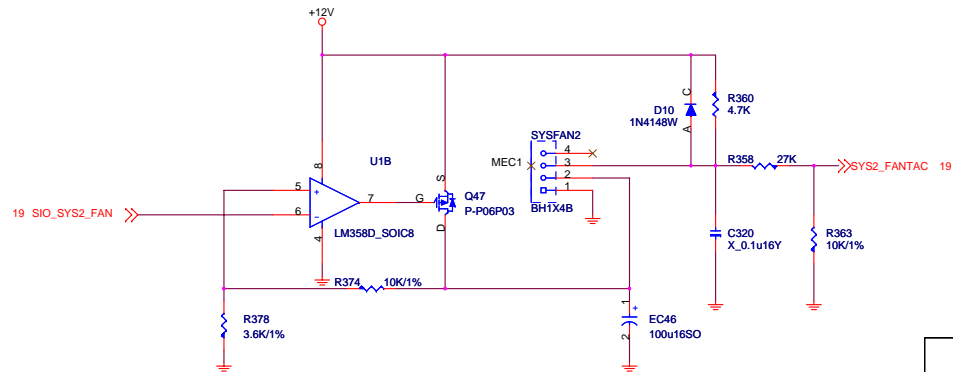
FAN-COUNTROL CIRCUIT



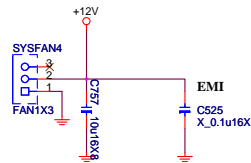
SYSTEM FAN3



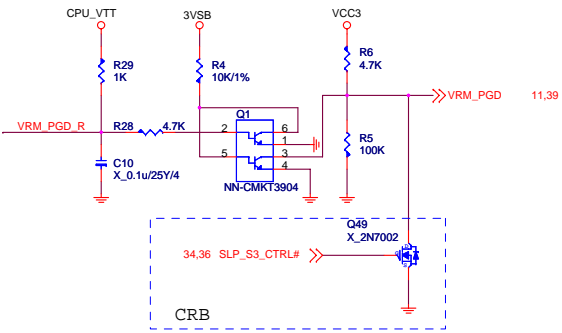
SYSTEM FAN2



SYSTEM FAN4



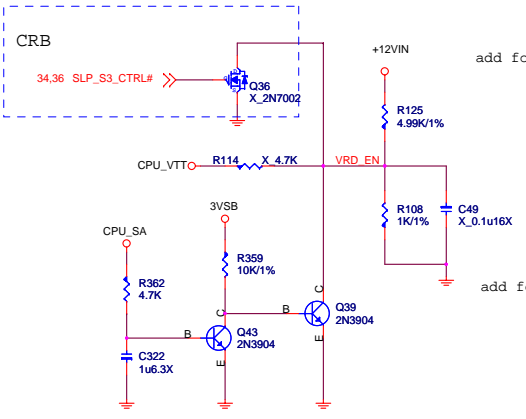
VRMPWRGD LEVEL SHIFT



3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND

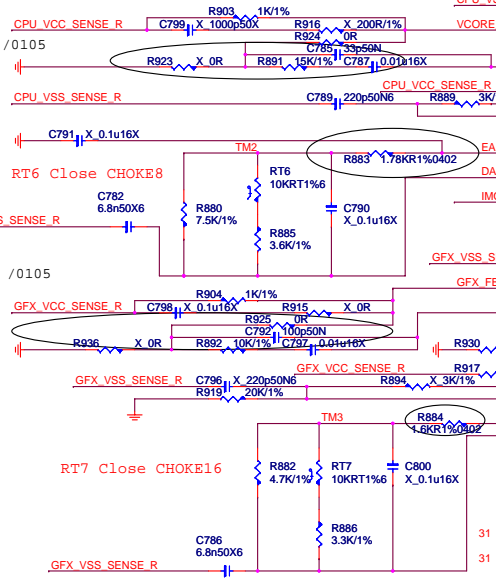
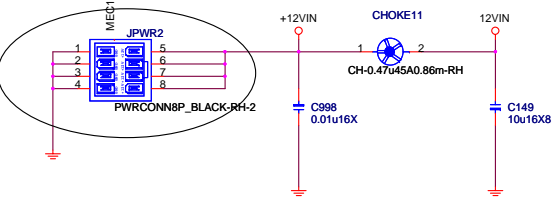
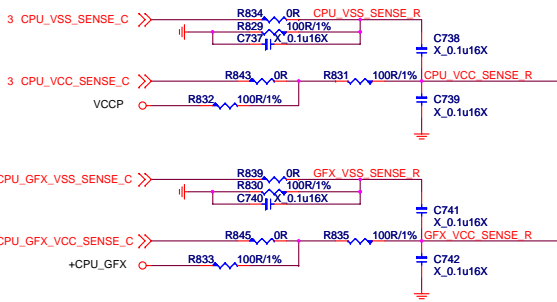
H_VIDSCLK
H_VIDSOUT

3 VID_ALERT# << VID_ALERT#
3 H_VIDSCLK << H_VIDSCLK
3 H_VIDSOUT << H_VIDSOUT



add for co_lay 1625Q+ /0105

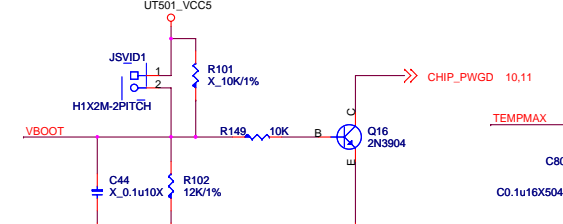
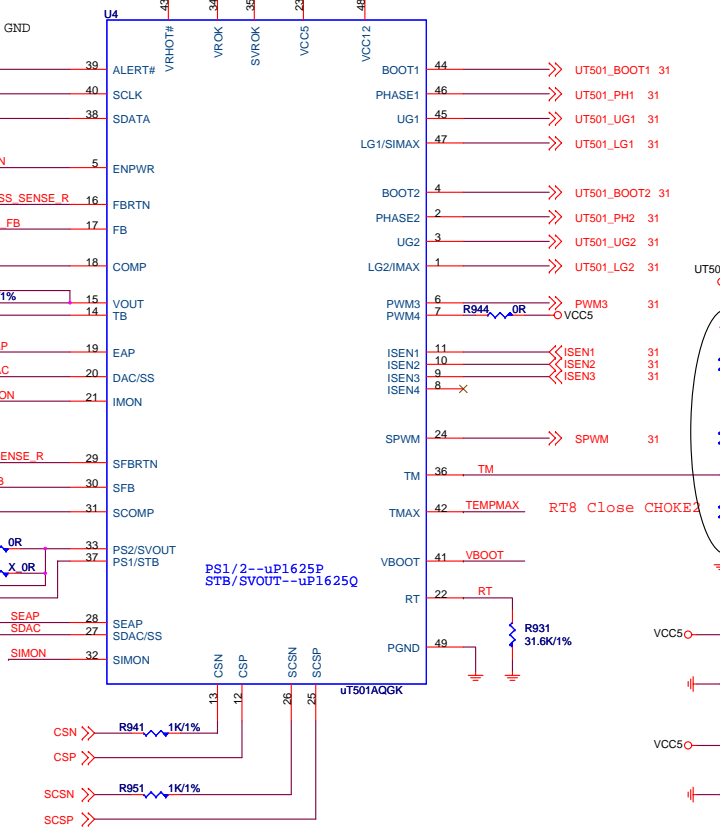
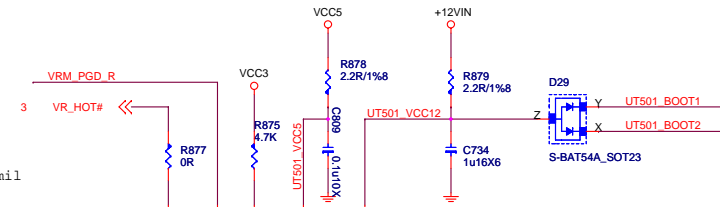
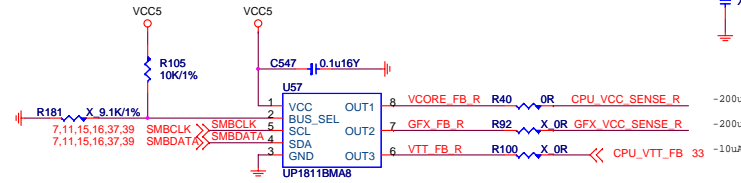
add for co_lay 1625Q+ /0105



UPI VOLTAGE CONSOLE

0x20: RH=10K, RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

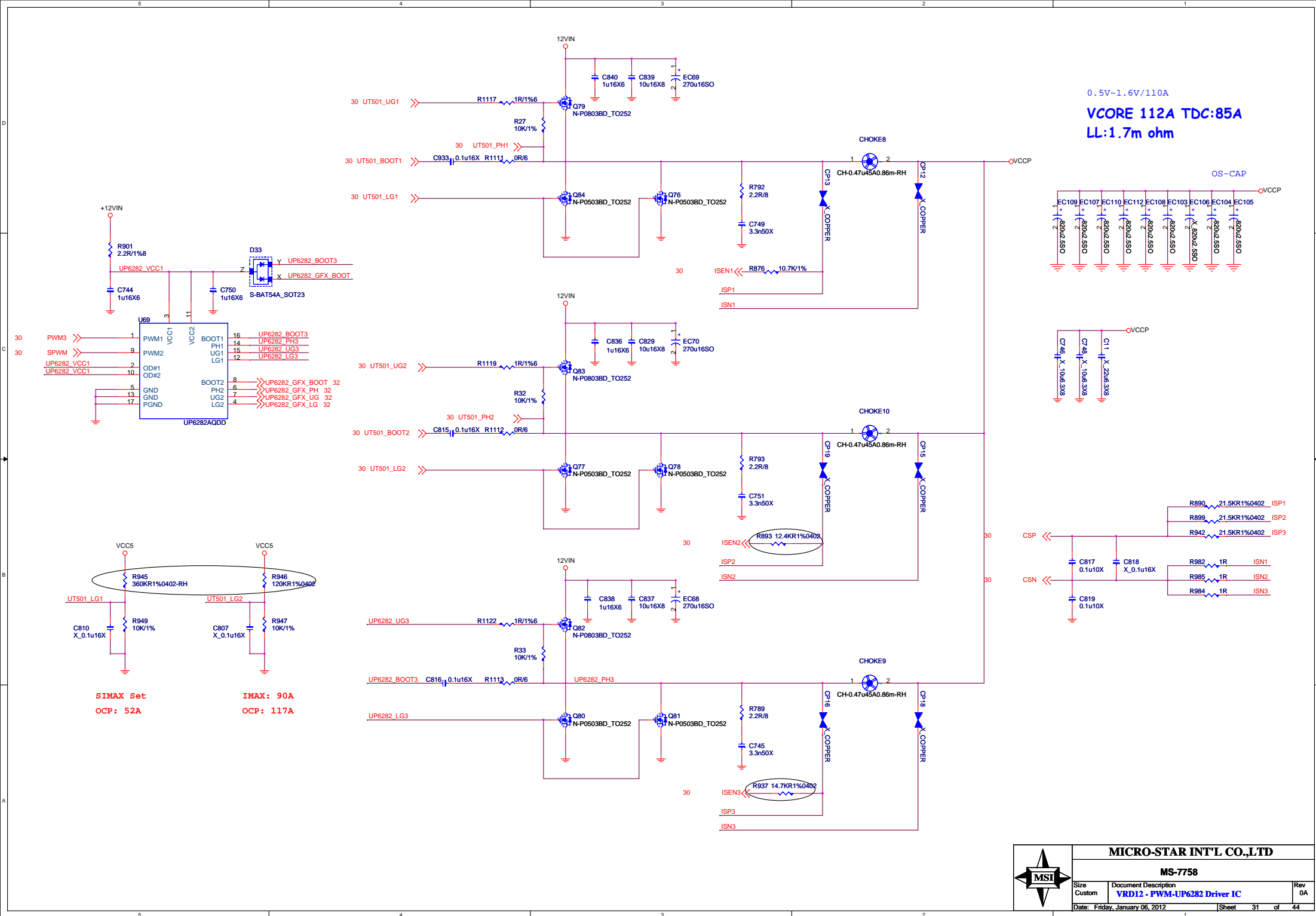


MICRO-STAR INT'L CO.,LTD

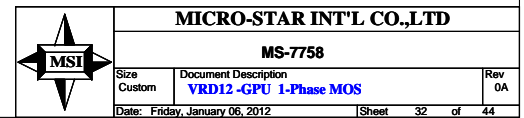
MS-7758

Size: Custom Document Description: VRD12 - PWM-UT501

Date: Friday, January 06, 2012 Sheet 30 of 44



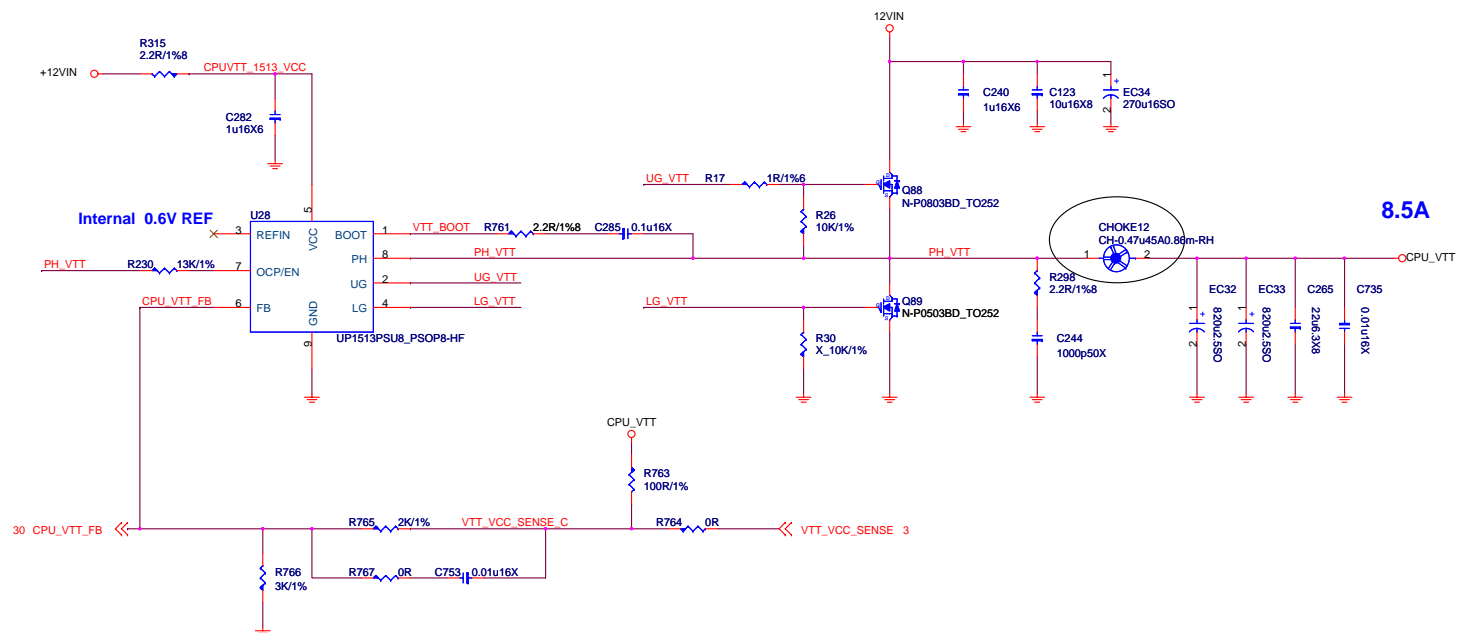
35A FOR CPU



8.5A FOR CPU

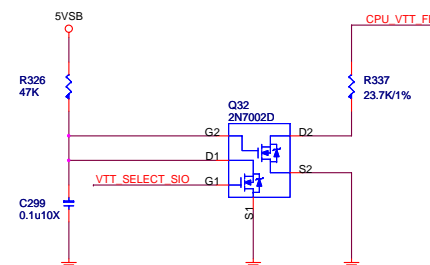
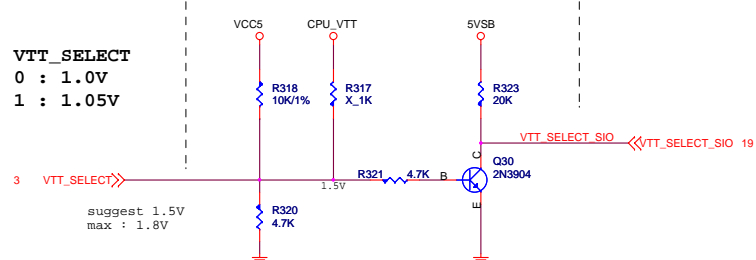
$$I_{ripple} = 1.92(v_{tt}) + 1.88(sa)$$

$$5 \times 1 = 5A > 3.8A$$



VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



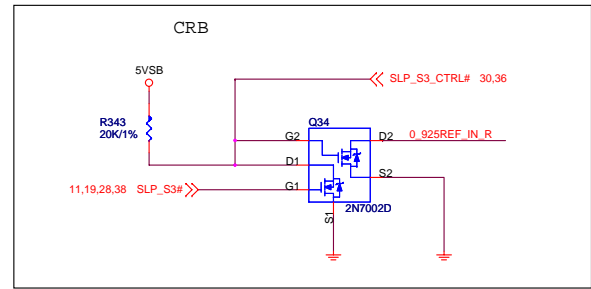
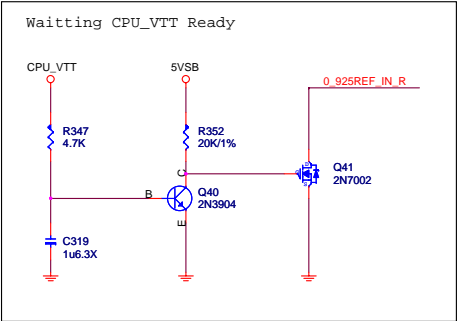
MICRO-STAR INT'L CO.,LTD

MS-7758

Size Custom	Document Description VTT POWER- uP1513- 1Phase MOS	Rev 0A
Date: Friday, January 06, 2012		Sheet 33 of 44

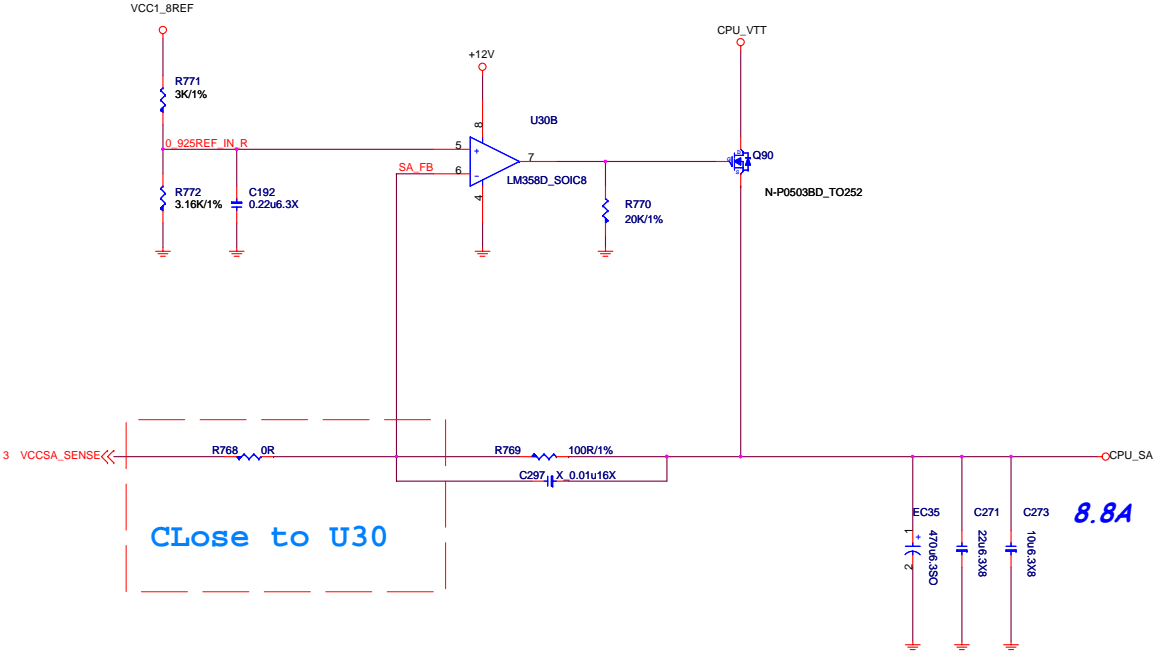
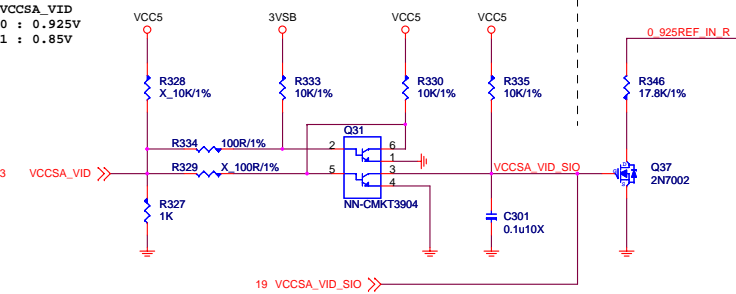
CPU_SA:0.925/0.85

SA Core =8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V



4.75A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

(OS-CON CAP)

C113 0.1u10X

EC16 470u6.3SO

EC19 470u6.3SO

CH-1.2u15A1.7u-RH

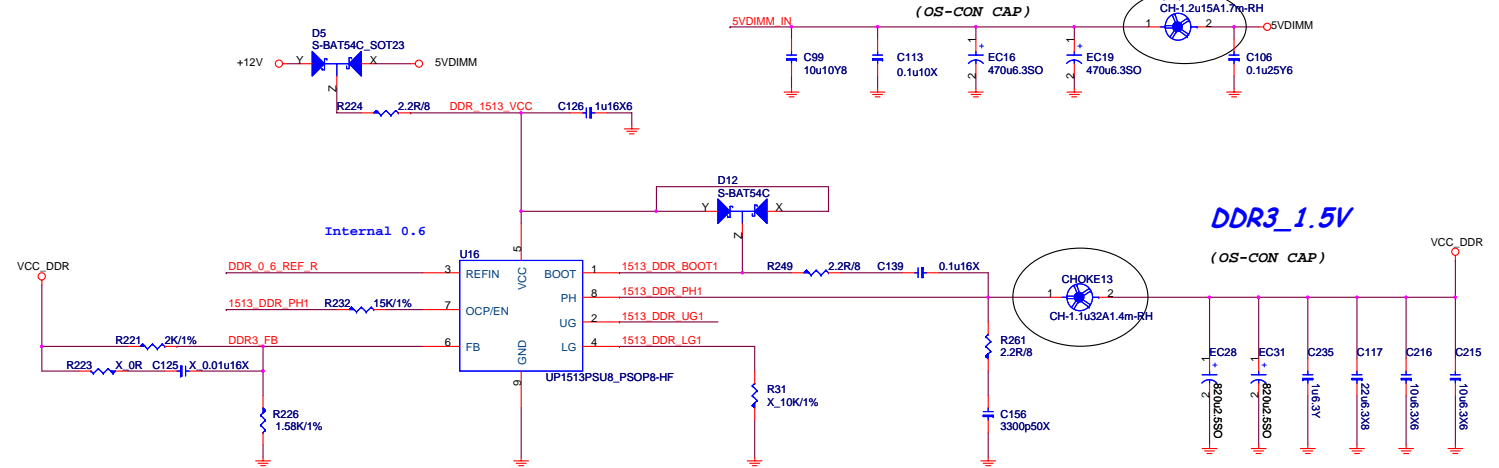
1 2

5V DIMM

C106 0.1u25Y6

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

```
DDR_OV2 = GPIO02(S/IO)
```



5VDDIMM_IN

1513_DDR_UG1

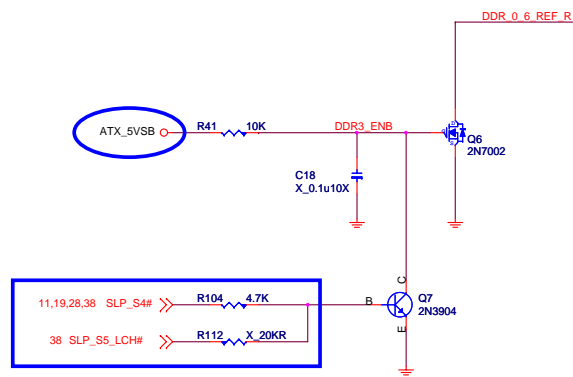
Q91
N-P0803BD_TO252

1513_DDR_PH1

Q92
N-P0503BD_TO252

1513_DDR_LG1

Q96
N-P0503BD_TO252

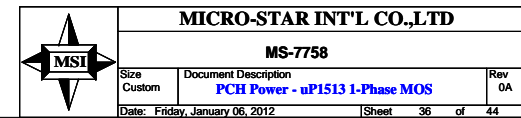


Size Custom	Document Description DDR Power -UP1513 1-Phase MOS
----------------	--

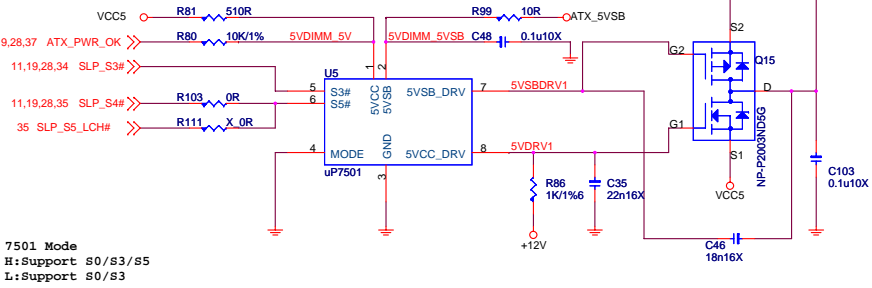
Date: Friday, January 06, 2012	Sheet 35 of 44
--------------------------------	----------------

1.8A FOR ME CORE

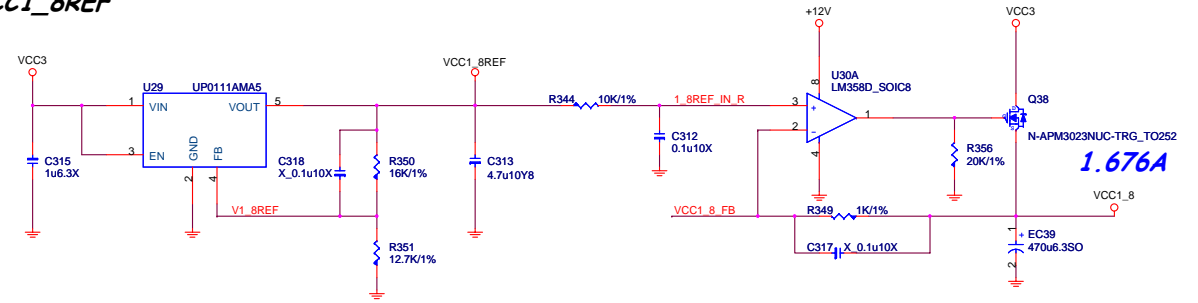
8A



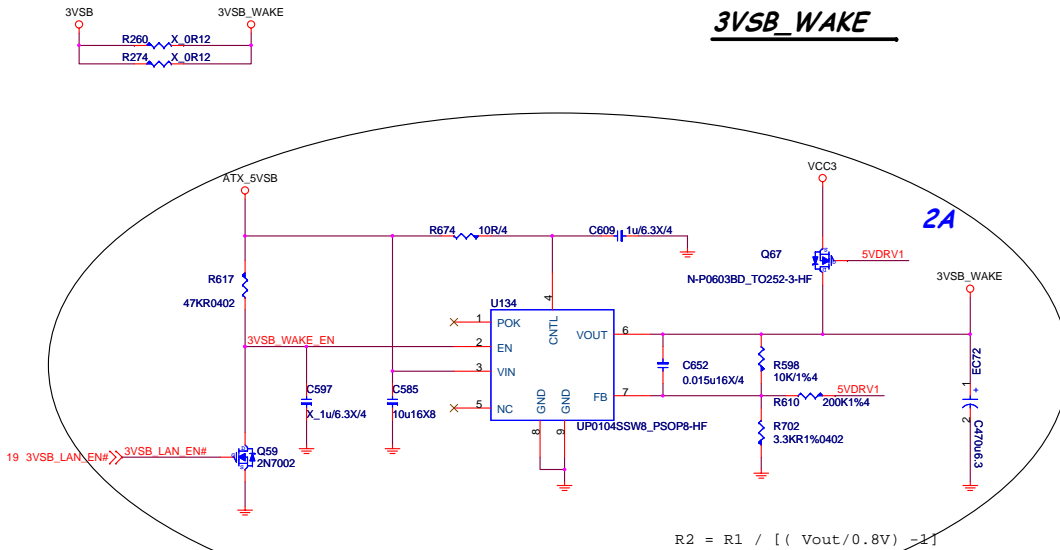
5VDIMM FOR DDR



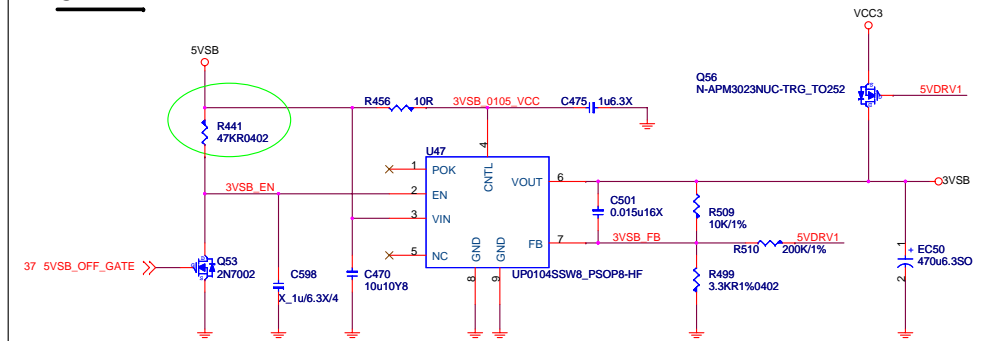
VCC1_8REF



3VSB_WAKE

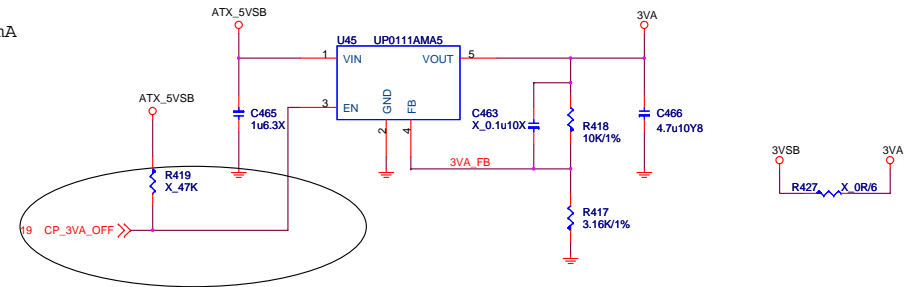


3VSB



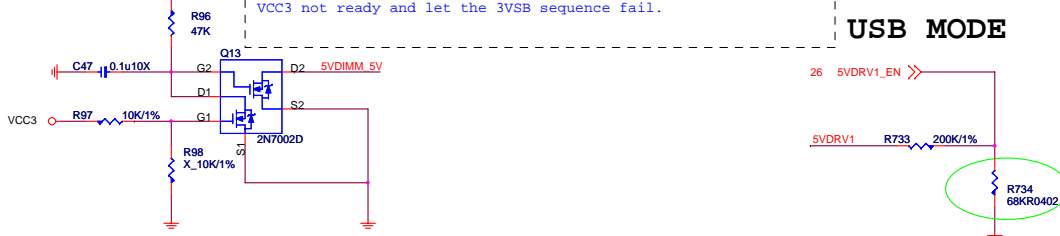
3VA

20mA

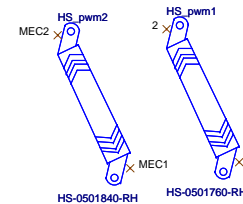


USB MODE

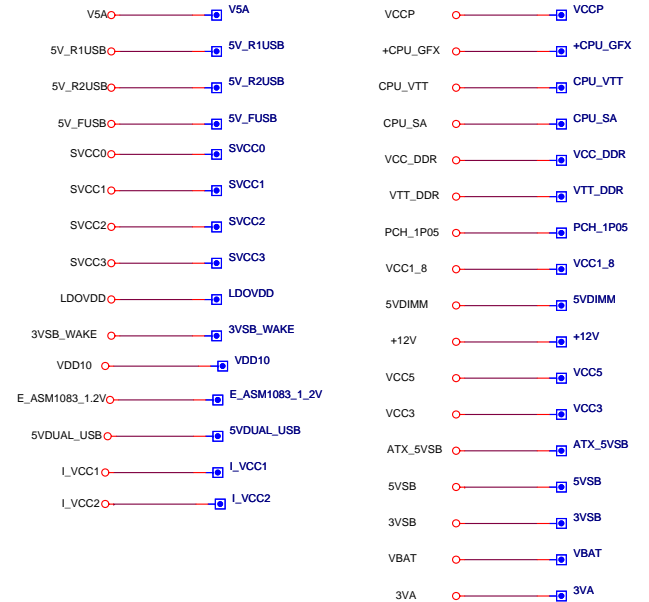
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



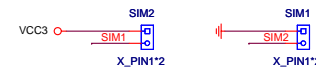
Mounting Holes



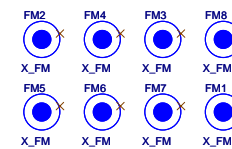
Voltage test point



Simulation



Optical Fiducial Marks-120



MICRO-STAR INT'L CO.,LTD

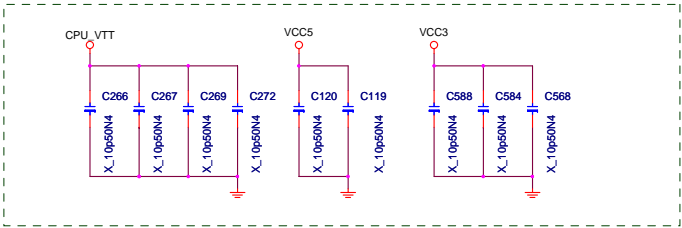
MS-7758

Size	Document Description
Custom	XDP / Manual Parts

Date: Friday, January 06, 2012	Sheet 39 of 44
--------------------------------	----------------

Rev
0A

EMI:cap. for signal return path



EMI

